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A NOVEL DESIGN OF REVERSIBLE 2:4 & 3:8 DECODER

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Abstract: Decoders are one of the most important circuits used in combinational logic. Different approaches have been proposed for their design. In this paper, a 2:4 decoder & have used it to build a 3:8 decoder has been designed to reduce power consumption, delay and quantum cost using reversible technology, which is then analyzed and comparative study has been done in account of the power consumption, delay, quantum cost and memory usage. Reversible logic is used to reduce the power dissipation that occurs in digital circuits by preventing the loss of information. The proposed 2:4 & 3:8 Decoders using reversible technology gives better results in terms of reversible parameters as compare to existing results. The decoder circuits are simulated using Xilinx ISE Simulator 14.4.

Keywords: Low power, Reversible logic, MFRG gate, 2:4 Decoder; Delay.

1. INTRODUCTION

Landauer [1] showed that the heat generated during computation is not due to the processing of bits, but due to the loss of information. Wiping of each bit of information causes a kTln2 amount of heat dissipation where k is the Boltzmann constant = 1.3805 * 10^23 J/K and T is the temperature in absolute scale. While this heat may be negligible for a single wipe of information, in modern VLSI design, where many chips are arranged in small region and millions of instructions are processed per second, the information loss and consequently the heat generation is formidable.

Bennett [2] later showed that this heat dissipation can be avoided by using reversible computation. This proof by Bennett has led to an extensive research on reversible logic. Most prominent applications of reversible logic are seen in quantum computation, low power CMOS design, nanotechnology and DNA computing.

Quantum networks are composed of quantum logic gates each gate performing an elementary unitary operation on one, two or more than two state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum arithmetic must be built from reversible logic components [3].

Quantum cost, delay and power consumption are the most important cost metrics of reversible computing. Number of gates is not a good measure of cost, since more than one gates can be taken together to form a new gate, thus reducing the gate count. Quantum gates involving many qubits are extremely difficult to build. Hence quantum cost is an important metric to build quantum gates. Quantum cost is the number of elementary quantum gates required to build the gate. 1*1 reversible gates viz. NOT gate have quantum cost 0 while 2*2 gates viz. Controlled-V, Controlled-V+, CNOT gate etc. have quantum cost 1 [4].

Design of combinational sequential circuits have been ongoing for some time. Various proposals are given for the design of adders, subtractions [5], multiplexers [6], decoders etc. Recently a new reversible SG gate [7]. In this paper, we have proposed a novel design of 2:4 decoder whose quantum cost is less than the previous design. A design has also been proposed to extend the 2:4 decoder to higher dimension i.e. 3:8 decoder using MFRG gate.

Rest of the paper is organized in the following way: Section 2 gives a brief introduction to the reversible gates used in this paper. In section 3 we give our proposed design of decoder, in section 4 the layout design of proposed decoders are discussed, in section 5 compare analysis of proposed decoders with the previous design is given. Section 6 concludes the paper.

2. BASIC REVERSIBLE GATES

Reversible gates are n*n logic gates where the input vectors I = I(i1; i2; : : : ; in) are mapped to the output vectors O = O(o1; o2; : : : ; on). The mapping is bijective, i.e., every input is mapped to an output and every output has a unique input mapped to it. Thus the outputs of reversible gates are permutations of the inputs. Fan-outs are not allowed in reversible circuit since they violate one-to-one mapping. Some basic reversible gates are introduced in this section.

2.1 NOT Gate

The simplest reversible gate is NOT gate. It is a 1*1 gate with quantum cost 0. NOT gate simply flips the input as shown in Fig. 2.1.

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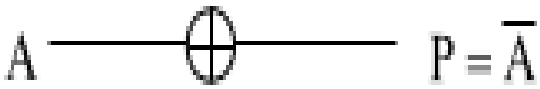

Fig. 2.1 NOT Gate

2.2 Controlled-V and Controlled-V+ Gate

Controlled-V and Controlled-V+ gates are 2*2 reversible gates with quantum cost 1. In Controlled-V gate, if the control signal A = 0, then the second input B passes unchanged.
Controlled-V and Controlled-V y have the following properties:
V * V = NOT
V * V+ = V+ * V = I
V+ * V+ = NOT
Hence Controlled-V is also called the square root of NOT gate. Quantum implementation of V and V+ are shown in Fig.2.2.

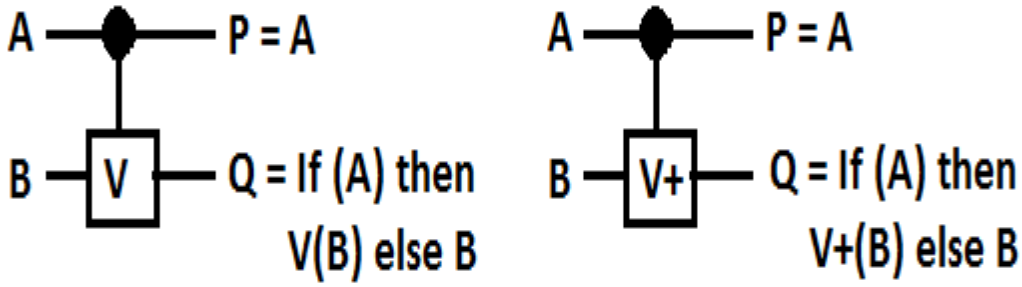

Fig. 2.2 Quantum Implementation of Controlled-V and Controlled-V+ Gate

2.3 MFRG Gate

Fig. 2.3 shows a 3*3 Modified fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P=A, Q=AB' ⊕ AC' and R=A'C ⊕ AB. Quantum cost of a Modified fredkin gate is 4.

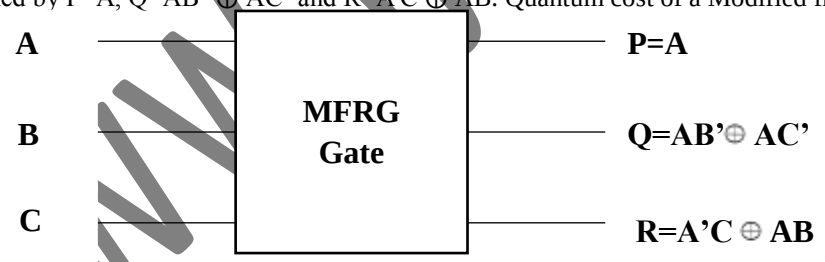

Fig. 2.3 MFRG Gate

3. PROPOSED DESIGN OF DECODERS

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a particular code. The N inputs can be a 0 or a 1, there are 2N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH.

3.1 2:4 Decoder

A design of 2:4 decoder using 3 Modified Fredkin gates is shown below. If x and y are the inputs to the decoder, then the four outputs will be xy, x'y, xy' and x'y'. The number of garbage output in this architecture is 1 and the number of constant inputs are 4. The existing 2:4 decoder was designed by the FRG reversible gates having quantum cost 5. The author proposed the 2:4 decoder using MFRG gate with low quantum cost of 4. The following figure shows the architecture of 2:4 decoder

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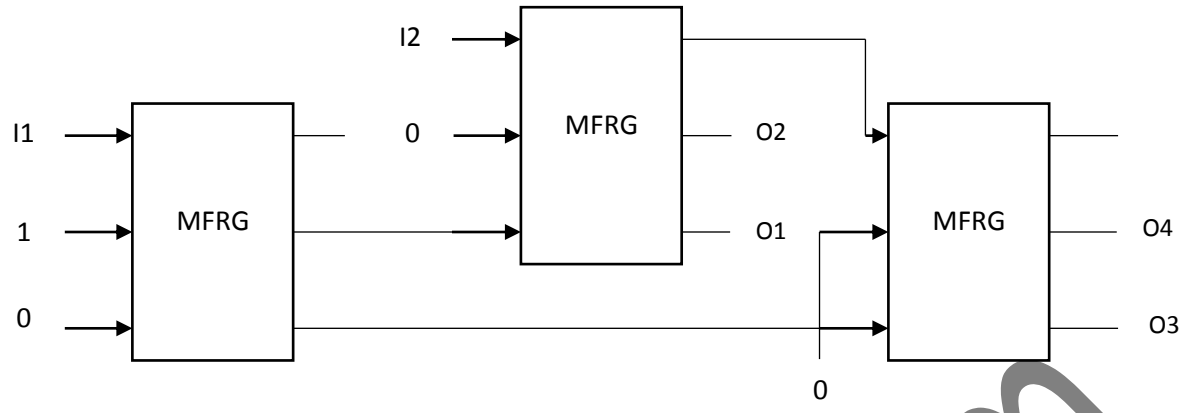

Fig. 3.1 Proposed 2:4 Reversible Decoder

3.2 3:8 Decoder

Henceforth, we shall call the 2:4 decoder as decoder block having two inputs and four outputs. A 3:8 decoder has the outputs x'y'z'; x'y'z; xy'z'; xy'z; x'yz'; x'yz; xyz'; xyz. So every output of the 2:4 decoder needs to be multiplied twice, once with z0 and then with z.

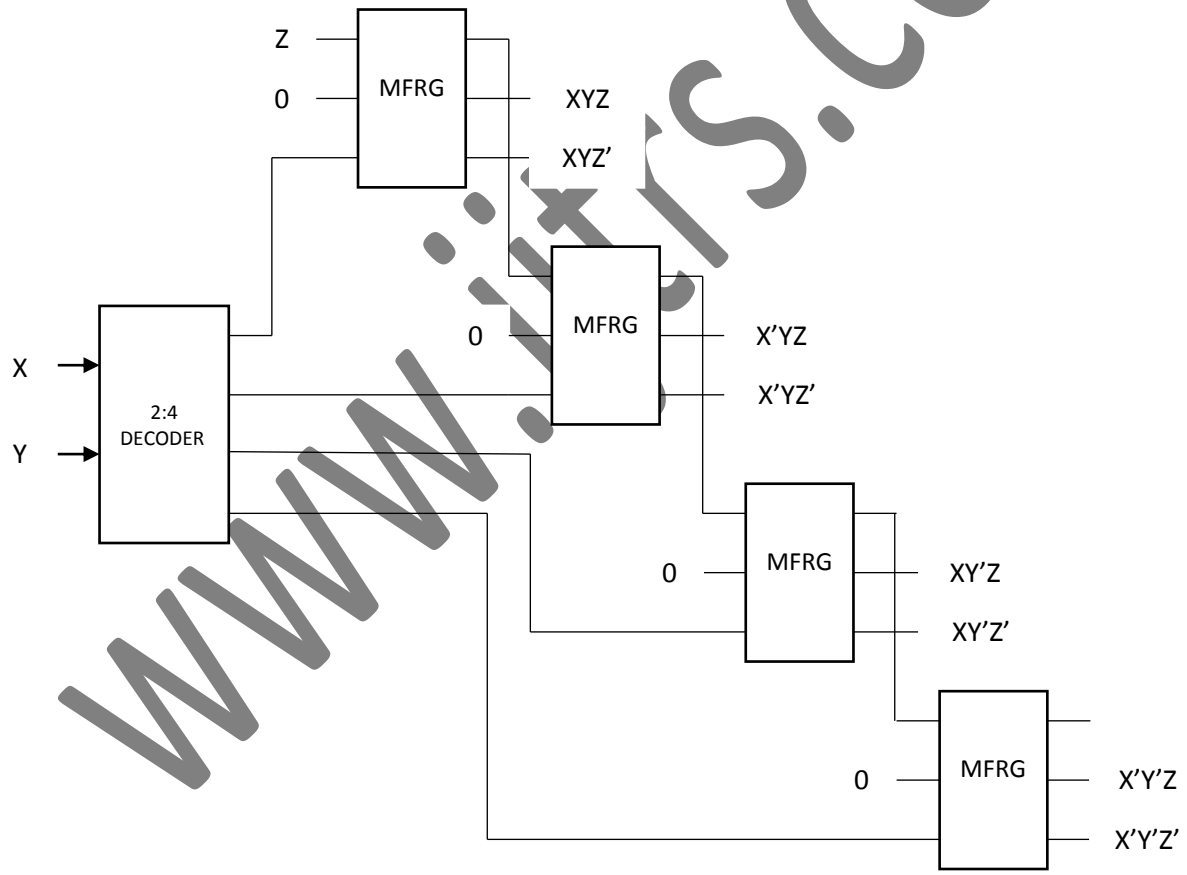

Fig. 3.2 Proposed 3:8 Reversible Decoder

A better model will be to use Modified Fredkin gate for higher dimension. Each Modified Fredkin gate is capable of performing two multiplications thus reducing the number of gates to 4 and garbage outputs to 1. The architecture is shown in Fig. 3.2.

4. LAYOUT SIMULATION

In this section, performance analysis of decoder has been presented. Designs simulations are done using Xilinx ISE 14.4 tool. The figure 4.1 & 4.2 shows the RTL views of various decoders

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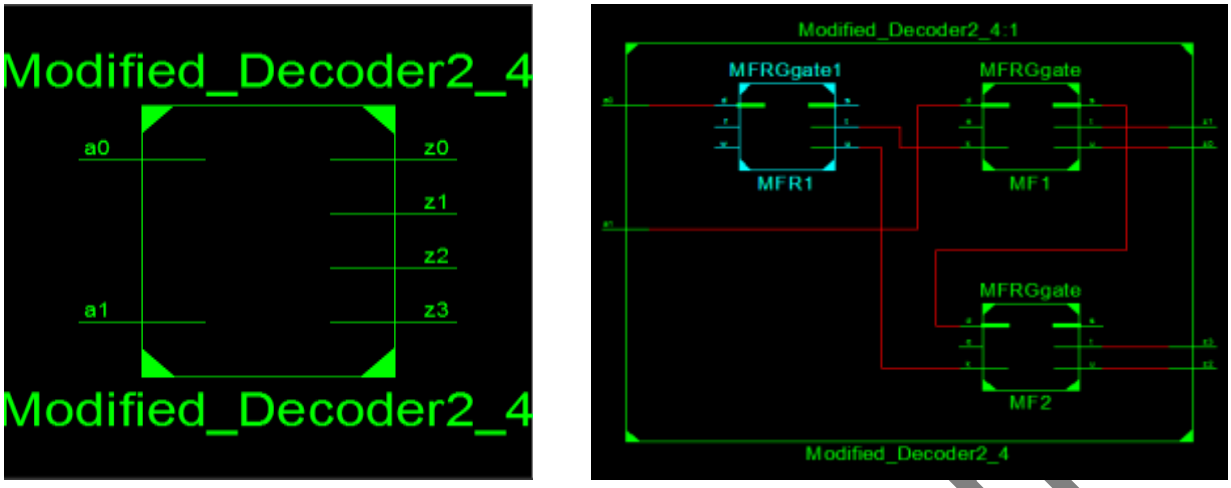

Fig. 4.1 RTL View of Proposed 2:4 Decoder

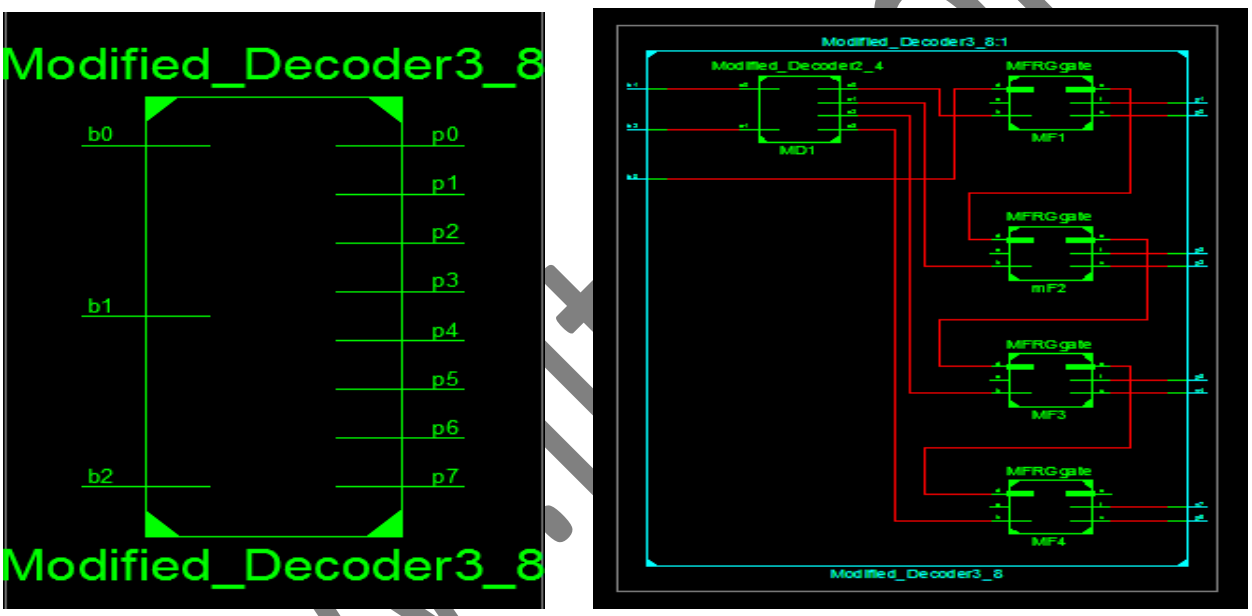

Fig. 4.2 RTL View of Proposed 3:8 Decoder

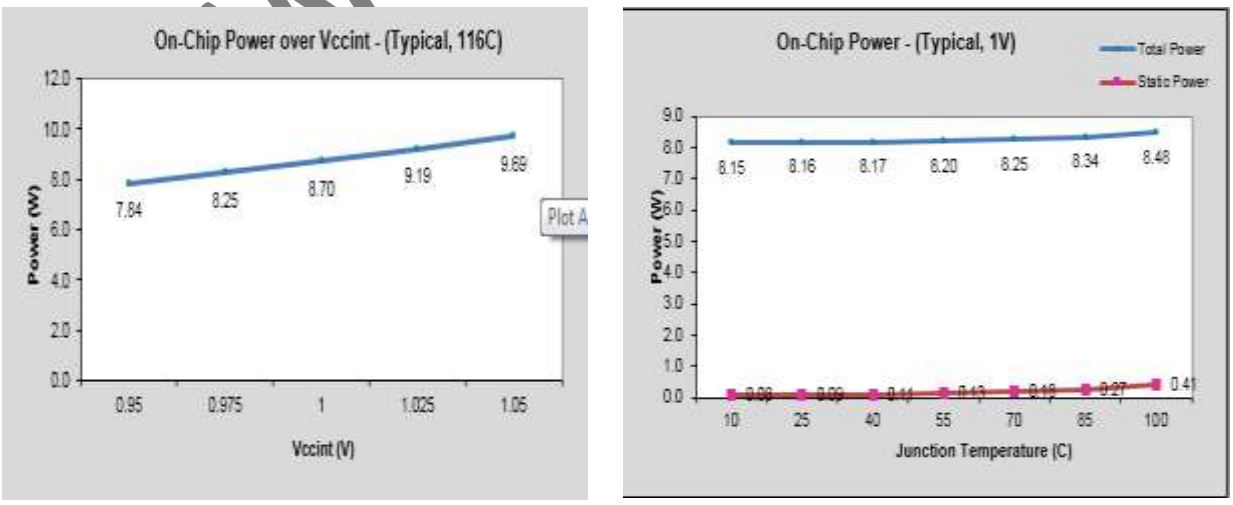

Fig. 4.3 Power Consumption Graph of Existing 2:4 Decoder [15]

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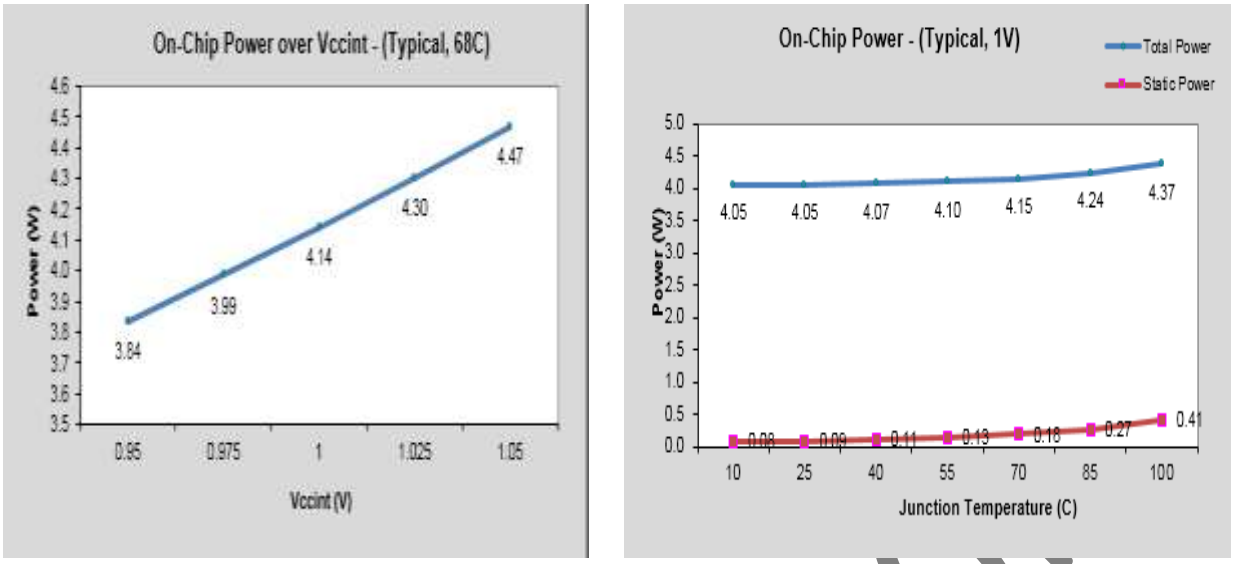

Fig. 4.4 Power Consumption Graph of Proposed 2:4 Decoder

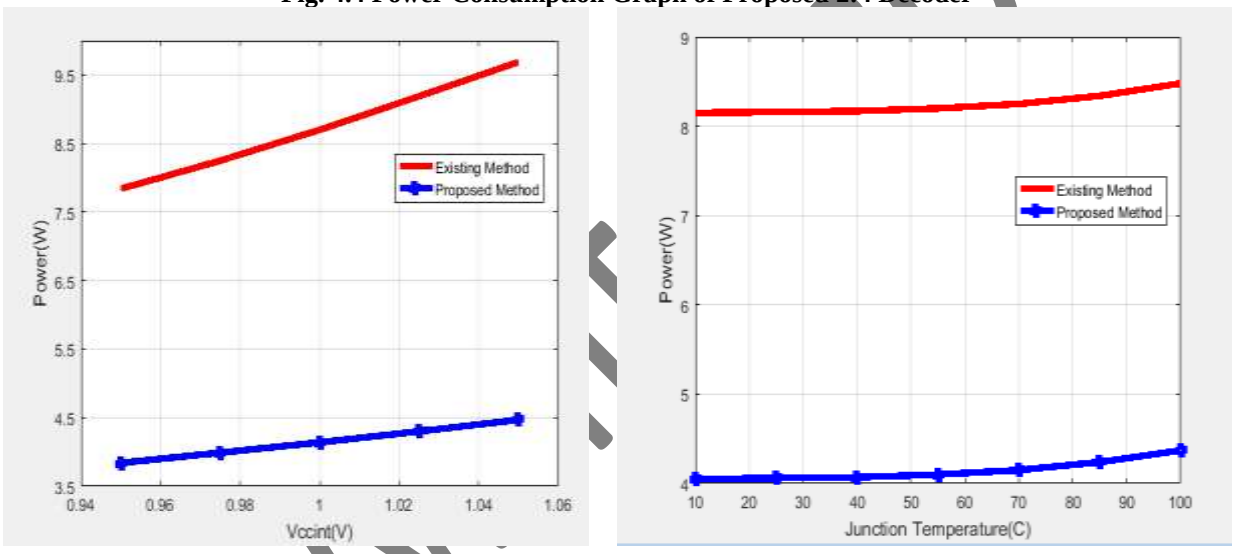

Fig. 4.5 Comparative Results of Power Consumption Graph for Proposed & Existing 2:4 Decoder [15]

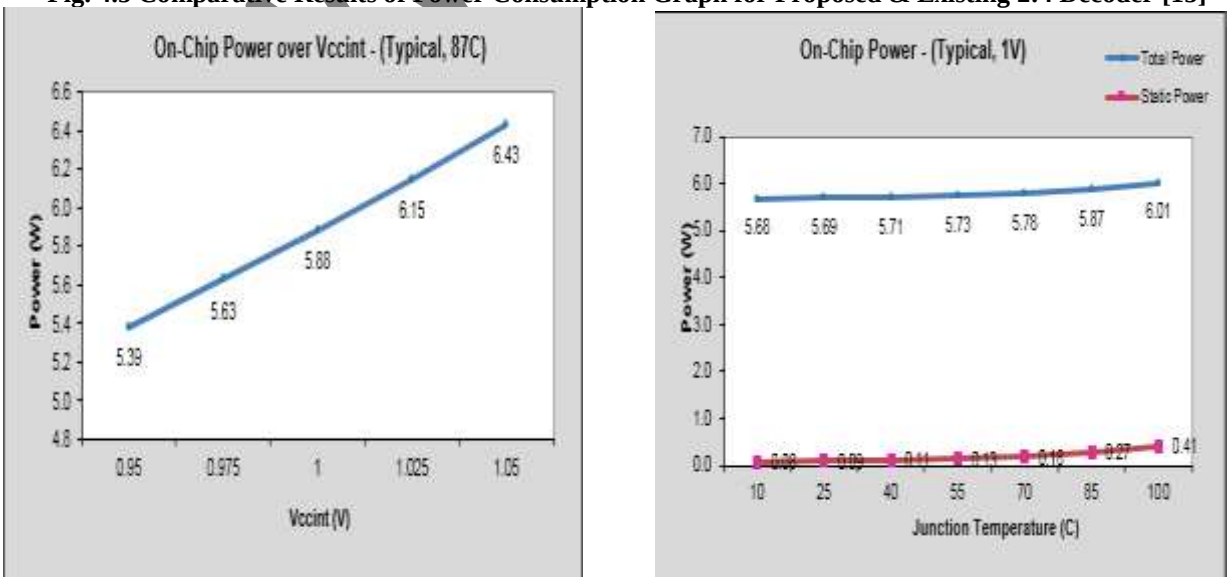

Fig. 4.6 Power Consumption Graph of Existing 3:8 Decoder [15]

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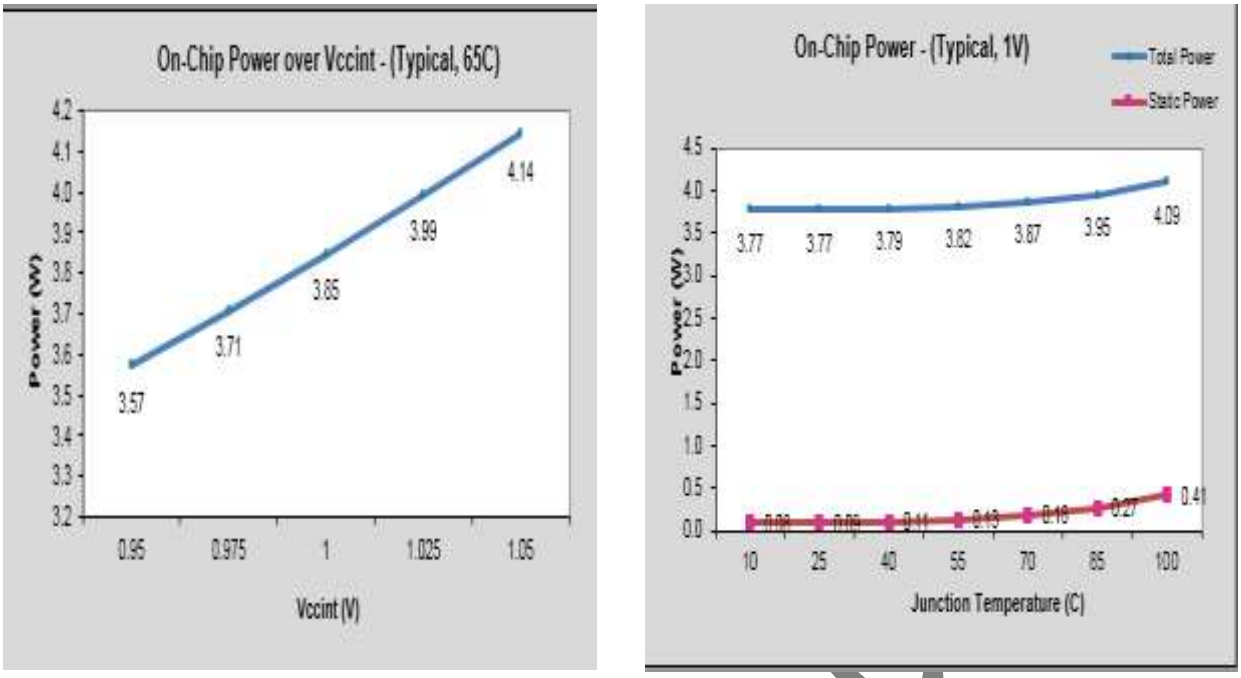

Fig. 4.7 Power Consumption Graph of Proposed 3:8 Decoder

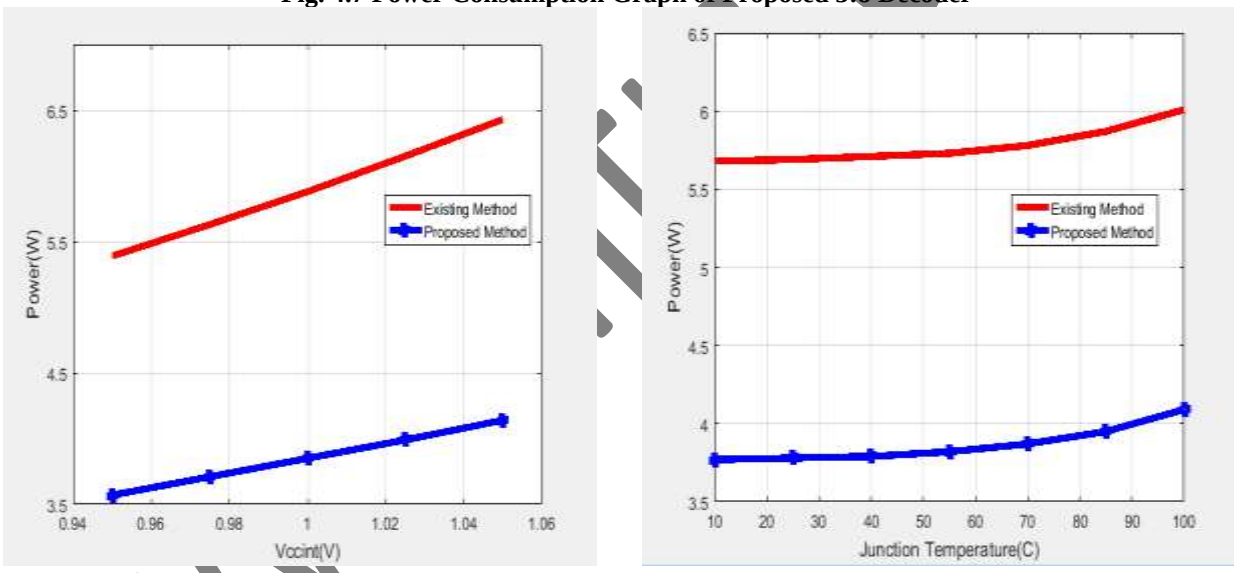

Fig. 4.8 Comparative Results of Power Consumption Graph for Proposed & Existing 3:8 Decoder [15]

In the fig. 4.5 the graph between the Vcc and Output power shows that the propose design consumes 4.14 Watt power while the existing design consumes 8.70 Watt power. Simillarly the graph between the Junction Temperature and Power shows that the propose design consumes 4.70 Watt power while the existing design consumes 8.70 Watt power.

In the fig. 4.8 the graph between the Vcc and Output power shows that the propose design consumes 3.84 Watt power while the existing design consumes 5.88 Watt power. Simillarly the graph between the Junction Temperature and Power shows that the propose design consumes 3.84 Watt power while the existing design consumes 5.88 Watt power.

Hence it cam be concluded that the proposed 2:4 and 3:8 decoders consumes less power as compared to the existing decoders.

5. IMPLEMENTATION & RESULTS

The table below gives the comparison of proposed work with the existing work in terms of quantum cost, power consumption, and delay and memory usage. We have compared our results with existing results of decoders by Ritajit Majumdar et al [15].

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Table-5.1. Comparison of Proposed Work with Existing Work

Parameters	2:4 Decoder	2:4 Decoder	3:8 Decoder	3:8 Decoder
	Existing Result [15]	Proposed Result	Existing Result [15]	Proposed Result
Quantum Cost	15	12	35	28
Power Consumption	8.704 W	4.141 W	5.882 W	3.847 W
Delay	5.362 ns	4.333 ns	5.607 ns	4.526 ns
Memory	250876 Kb	240300 Kb	250684 Kb	24864 Kb

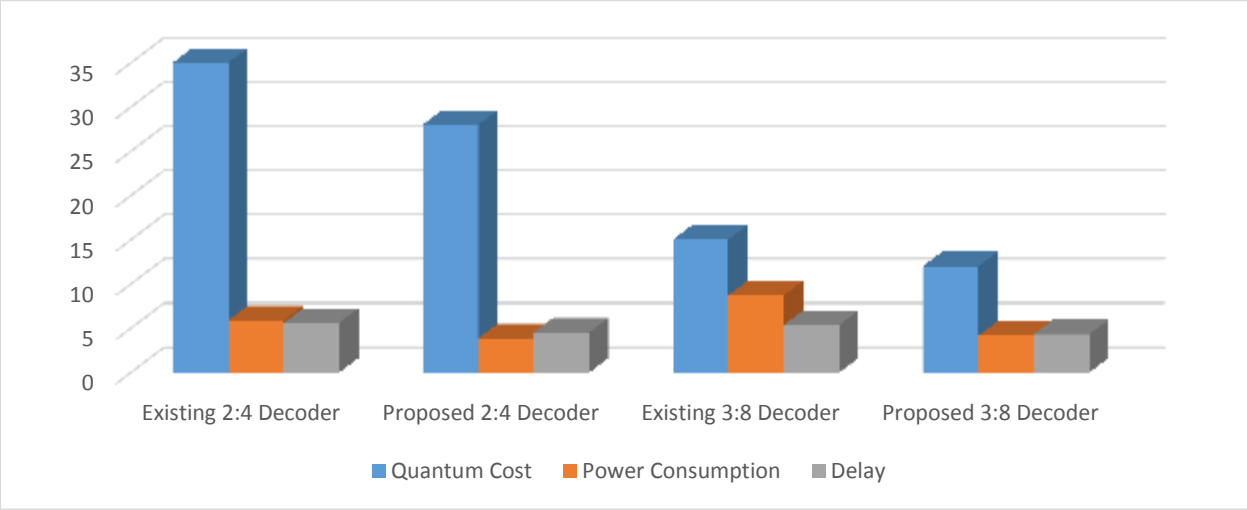

Fig. 5.1 Comparative Analysis for Proposed & Existing 2:4 & 3:8 Decoder [15]

The fig. 5.1 shows the comparative analysis results for quantum cost, power consumption, and delay and memory usage for various designs. The comparative results shows that our proposed designs are more efficient as compared to existing designs in terms of quantum cost, power consumption, delay and memory usage.

CONCLUSION

In this article, we have proposed a novel design of 2:4 decoder and have used it to build a 3:8 decoder. The increase in the number of Fredkin gates is exponentially higher for increase in a single input. Though for n inputs, the number of outputs is 2n. Hence, from the point of view of the number of outputs, the increase in gates is linear. However, by using any other gates like Toffoli, Peres or TR gate, the number of gates will be twice as high and hence the quantum cost will be nearly twice. The number of garbage outputs also increases in the same manner since each Fredkin gate has one garbage output for this architecture. Low power consumption and quantum cost is obtained using proposed logic for designed 2:4 & 3:8 Decoder.

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