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COMMON MODE VOLTAGE REDUCTION IN DIODE-CLAMPED MLI USING SPWM TECHNIQUES

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Abstract- The three-level Neutral-Point-Clamped (NPC) Voltage Source Inverter (VSI) is being employed in industrial and traction applications, static VAR compensation systems, active filtering and utility interconnection applications. Various strategies including carrier-based PWM schemes and Space Vector Modulation (SVM) based PWM schemes have been proposed to balance the NP voltage. The inverters having an odd number of levels will generate zero common-mode voltage by switching among certain states using space vector PWM (SVPWM) techniques. Therefore, motor bearing currents will be eliminated and conducted EMI will be reduced. Three-level inverters generate lower CMV as compared to conventional two-level inverters. The carrier based techniques are presented to control the magnitude and rate of change of common mode voltages in multilevel inverters using different structures of sine-triangle comparison method such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Common Mode Voltage off-set signal addition methods. Simulation results presented confirm the effectiveness of the proposed techniques to control the common mode voltages or reduced the common mode voltage.

Keywords: CMV, NPC, VSI, SVPWM, SVM, EMI and ASD.

1. INTRODUCTION

Recently, multilevel inverters have been found wide spread acceptability in medium and high voltage applications. Multi-level inverters have the advantage of producing high voltage high power with improved power quality of the supply. It also eliminates the use of problematic series-parallel connections of switching devices. However, multilevel PWM inverters generate common mode voltages as in the case of conventional 2-level inverters. The problem of common mode voltage generation in multilevel inverters has been studied extensively during last decade [1-5]. Common mode voltages are generated due to shaft voltages, circulating leakage currents through parasitic capacitance between motor windings, rotor and frame. The number of current spikes and magnitude of common mode voltage is determined by dv/dt and number of commutations. Several methods have been suggested for solving this problem. Some methods are based on additional circuit like filters. Other methods use advanced modulation strategies avoiding the generation of common mode voltages. But, these methods work at higher switching frequency, thus increasing the losses [1]-[3]. Various multilevel inverter control techniques, using sine-triangle comparison, for harmonic reduction have been reviewed in [4]. But the issue of common mode voltage control was not covered. Opportunities of harmonic reduction in cascaded multilevel inverters were investigated in [5-6] using carrier based PWM techniques. Conventional multilevel SPWM techniques generate a significant amount of common mode voltage which may be around the dc voltage level.

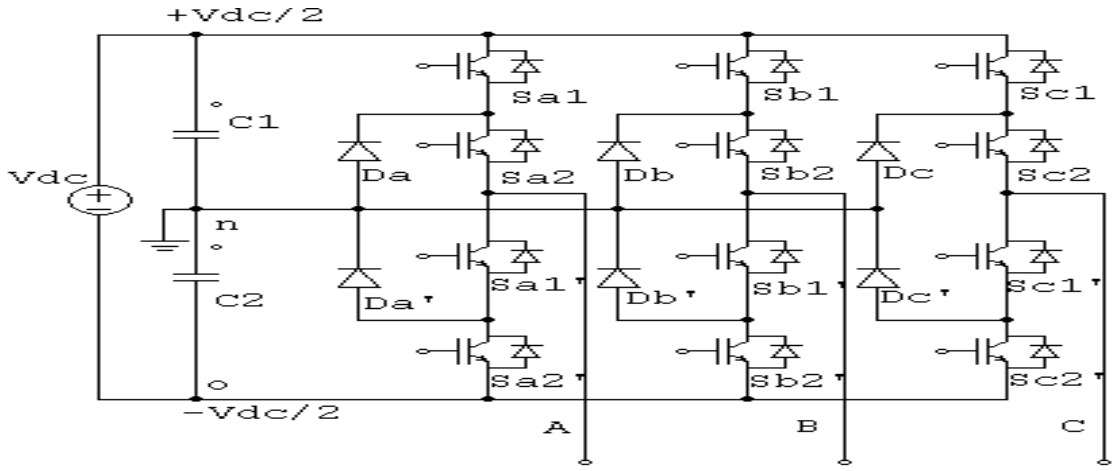

Fig. 1.1 Thee Phase Diode-Clamped Three level Inverter

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Another problem which NPC inverter faces is neutral point potential (NPP) variation due to voltage unbalancing between two capacitors. Due to the variation in NPP, excessive high voltages may be applied across switching devices. Several methods have been investigated to control the NPP variation and neutral point current [7-10]. A neutral point voltage regulator has been modelled and designed in [10]. But it works at 5 kHz switching frequency resulting in high switching losses. In this paper, a NPP regulator is presented which works at low switching frequency of 2 kHz. This paper also investigates the possibilities of using different multilevel SPWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD) and Common Off-set voltage addition method (Bias method) to reduce the common mode voltages in 3-level diode clamped inverter. Results show drastic reduction in THD using modified SPWM methods. At the same time common mode voltages are also controlled up to nearly half of the magnitude as compared to conventional multilevel SPWM methods. Neutral point potential variation is also controlled by closed loop PI regulator. This regulator provides capacitor voltage balancing and harmonics reduction in load voltage and current below IEEE-519 standard.

2. OPERATION OF 3 - LEVEL SPWM

Fig. 1.1 shows the very popular topological structure of diode clamped 3-phase, 3-level inverter considered here for study. The switching states of the inverter are shown in Table I for one leg. It gives the output pole voltage V_{AO}, output line voltage V_{AB} and switch state. Switch state '1' means 'on' and '0' means 'off'. This switching pattern can be achieved by means of different multilevel control strategies such as square wave switching, sine-triangle comparison method (SPWM), space vector modulation (SVM), selective harmonic elimination technique, hysteresis current control, sigma-delta modulation etc. Of these methods, sinusoidal pulse width modulation (SPWM) is the simple and cost effective method to implement, therefore considered here.

Table-1.1switching States of 3-Level Diode Clamped Inverter

V_{AB}	**Output Pole Voltage (V_{AO})**	**Switch States**			
		S_{a1}	**S_{a2}**	**$S_{a1}^{!}$**	**$S_{a2}^{!}$**
$-V_{dc/2}$	0	0	0	1	1
0	$V_{dc/2}$	0	1	1	0
$V_{dc/2}$	V_{dc}	1	1	0	0

SPWM technique is again sub divided into following categories:

- Phase Disposition (PD) method,
- Phase Opposition Disposition (POD) method,
- Phase Shifted (PS) method,
- Hybrid method,
- Third Harmonic Injection (THI) method.

Basic principles of pulse generation for 3-level PD and POD SPWM techniques are shown in Fig. 22 and 3. Fundamental frequency three-phase sinusoidal reference waves V_a , V_b and V_c are compared with two high frequency triangular carrier waves 'carrier 1' and 'carrier 2'. Each intersection gives rise to the control pulses for switching devices of inverter. The reference sinusoidal waves can be represented by,

$$\left.\begin{aligned} Va &= V_m \sin(\omega t) \\ V_b &= V_m \sin(\omega t - 120°) \\ V_c &= V_m \sin(\omega t - 240°) \end{aligned}\right\} \quad (1)$$

PD and POD SPWM techniques have been selected for study without and with addition of common mode voltage off-set as shown in Fig. 2.2 to Fig. 2.5. Common mode voltage or zero sequence voltage in output voltage of inverter can be represented by,

$$V_{cm} = (V_a + V_b + V_c) / 3 \quad (2)$$

Where, V_a, V_b, V_c are the phase voltages of inverter. This voltage is around 150-200 volts (peak) in conventional 2-level inverters for a dc voltage of 200 volts. To reduce it, following common mode off-set voltage is to be added,

$$V_{offset} = [\min(V_a, V_b, V_c) + \max(V_a, V_b, V_c)] / 2 \quad (3)$$

Therefore the new reference or modulation wave becomes,

$$V^* = V(a, b, c) + V_{offset} \quad (4)$$

Where, V(a, b, c) is given by equation (1). Fig. 2.4 and Fig. 2.5 give the reference 3-phase waves as obtained from equation (4). The 'max', 'min', one phase voltage vr and off-set voltage signals, as obtained from equation (3) and (4), are shown in Fig. 2.6 for PD SPWM case.

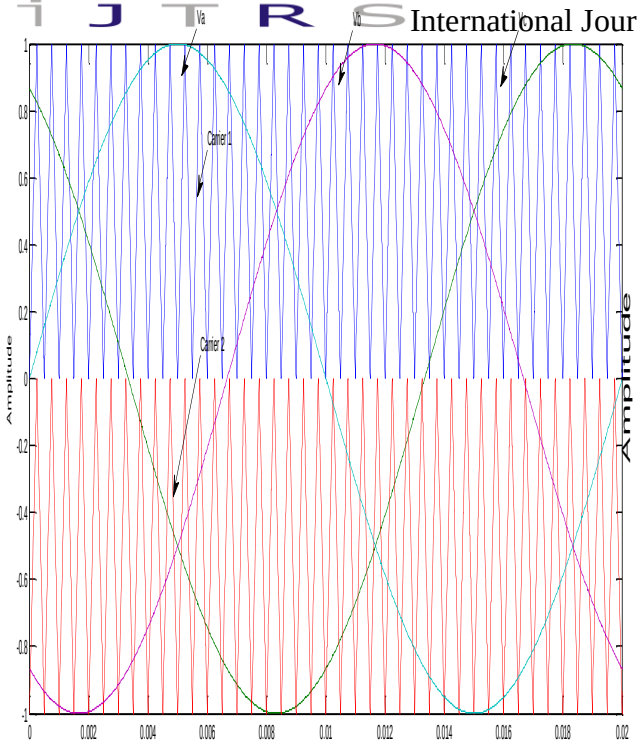

Fig. 2.2 Modulation and Carrier Waveforms with PD SPWM Technique

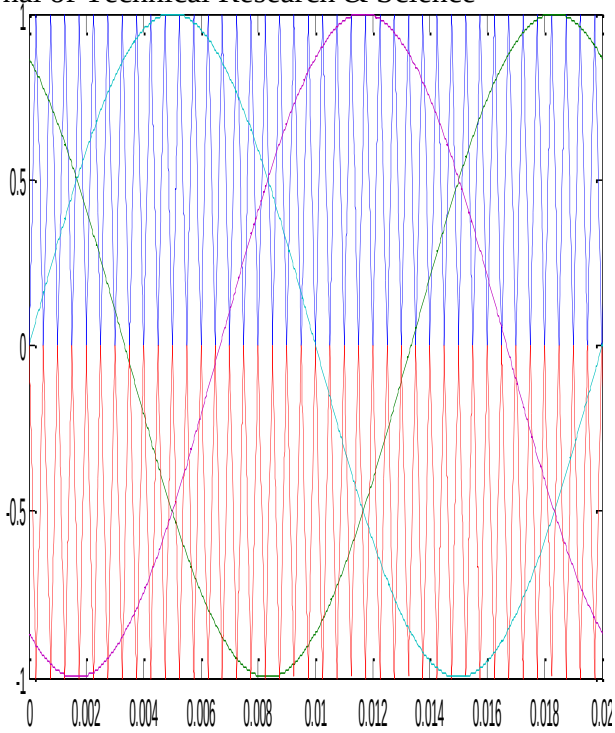

Fig. 2.3 Modulation and Carrier Waveforms with POD SPWM Technique

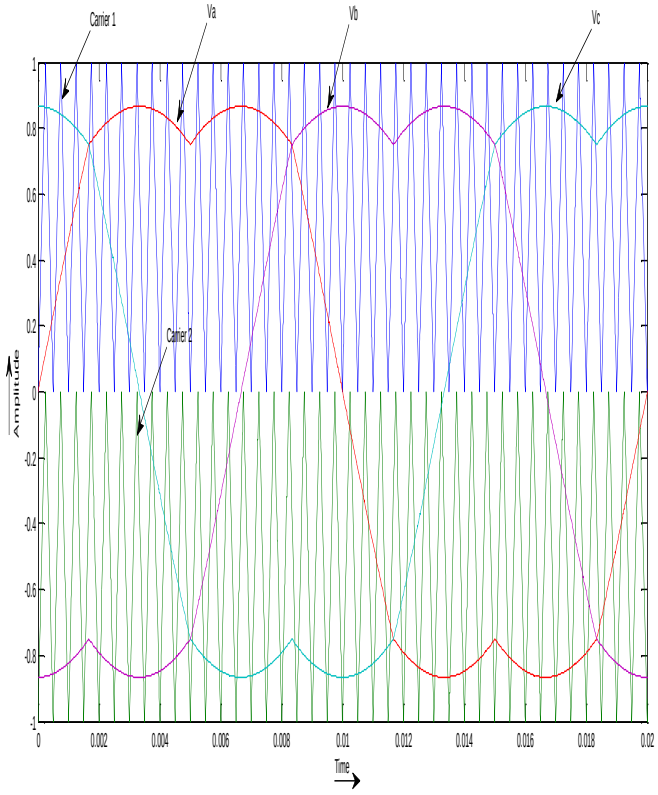

Fig. 2.4 Modulation and Carrier Waveforms with Addition of Common Mode off-set Voltage in PD SPWM Technique

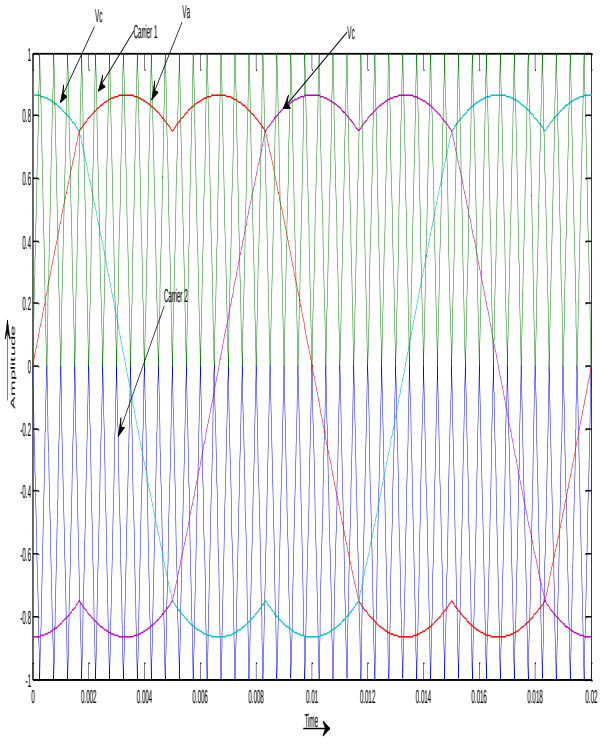

Fig. 2.5 Modulation and Carrier Waveforms with Addition of Common Mode off-set Voltage in POD SPWM technique

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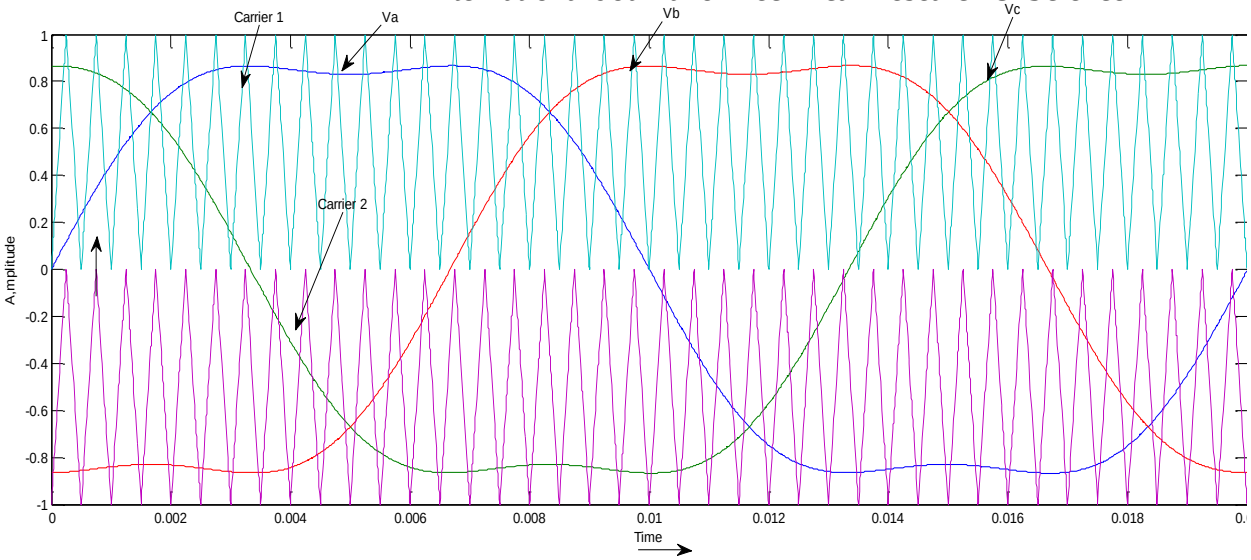

Fig. 2.6 Signals 'Vmax', 'Vmin', 'Va' and off-set Voltage 'V_{offset}' in PD SPWM Technique with Addition of offset Voltage to the Reference Signals

3. DESIGN OF NEUTRAL POINT POTENTIAL REGULATOR

Fig. 3.1 shows the closed loop scheme of proportional integral (PI) neutral point potential (NPP) regulator. The proposed PI voltage regulator aims to stabilize the dc link voltage to control neutral point potential variation by controlling the charging and discharging of upper and lower dc bus capacitors without dc capacitor voltage sensing. Three phase inverter output voltages are sensed and converted into per unit system. These per unit voltages are converted into dqo axis using following 3-phase to two-phase conversion,

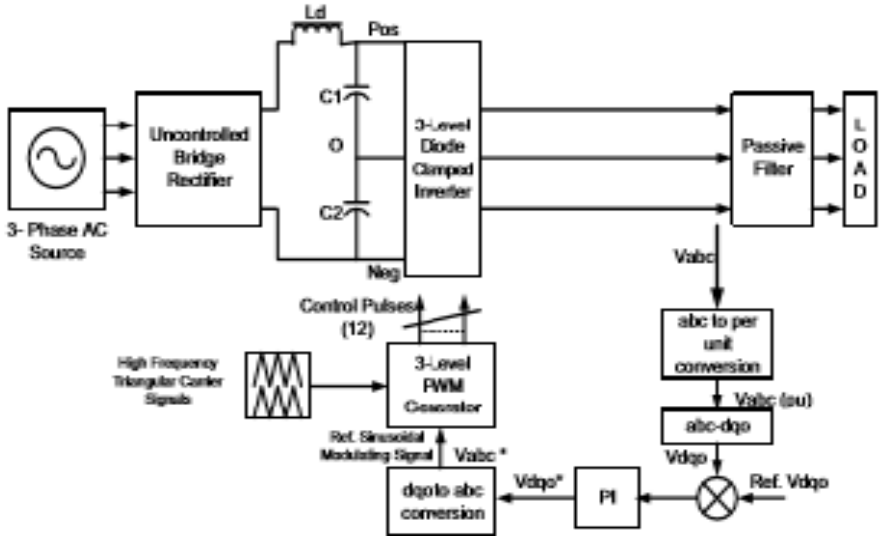

Fig. 3.1 Block diagram of Closed Loop Voltage Regulator

$$Vd = 2/3\,[Va \sin(wt) + Vb \sin(wt\text{-}120^0) + Vc \sin(wt\text{-}240^0)],$$
$$Vq = 2/3\,[Va \cos(wt) + Vb \cos(wt\text{-}120^0) + Vc \cos(wt\text{-}240^0)],$$
$$Vo = (Va + Vb + Vc)/3 \quad (5)$$

These dqo voltages, Vdqo, are compared with set values of dqo voltages Vdqo*. It results in voltage error which is processed through a proportional-integral (PI) controller to generate two axis command signals Vdq. Then three phase reference voltage signal for PWM generator is synthesized using following two-to-three phase conversion,

$$Va = [Vd \sin(wt) + Vq \cos(wt) + Vo],$$
$$Vb = [Vd \sin(wt\text{-}120^0) + Vq \cos(wt\text{-}120^0) + Vo],$$
$$Vc = [Vd \sin(wt\text{-}240^0) + Vq \cos(wt\text{-}240^0) + Vo] \quad (6)$$

Amplitude modulation index, m, is defined as,

$$m = \text{sqrt}\,(V^2d + V^2q) \quad (7)$$

And the gain of PI controller is,

$$G = Kp + [Ki * Ts / (Z-1)] \quad (8)$$

Values of Kp, Ki and limits of integration are tuned to achieve fast response of modulation index and to reduce NPP variation below 2%. Output of 3-level PWM generator block is the 3phase sinusoidal reference signals to be applied to the PD SPWM scheme as discussed in previous section.

4. SIMULATION RESULTS

A simulation model has been developed in Mat lab environment. Simulation parameters are given in Appendix I. Fig. 4.1 and Fig. 4.2, show the waveforms and harmonic spectrum of line voltage with PD SPWM technique and POD SPWM technique. It is observed that fundamental voltage is increased from 173.2 volts to 181.2 volts with reduction in % THD from 29.34% to 2.00%. Switching frequency used is 1 kHz. Table II gives the % THD and fundamental value of line voltage (V_{1ab}) and current (i_{1a}) without and with filter. From this table, it is clear that the fundamental voltage increases with filter and maintaining the low THD, well below the IEEE-519 standard.

Fig. 4.3 gives the common mode voltages with normal and offset addition PD and POD SPWM techniques. It is clear from the Fig. 4.3 that peak of the common mode voltage (Vcm) is less sharp in the case of Fig. 10 (c) and amplitude is reduced in PD SPWM to POD SPWM. Also frequency of Vcm is reduced in Fig. 10(d) as compared to its counterpart in Fig. 10(b). Therefore, POD SPWM technique will be advantageous in view of the common mode voltage amplitude and frequency stress on motor windings.

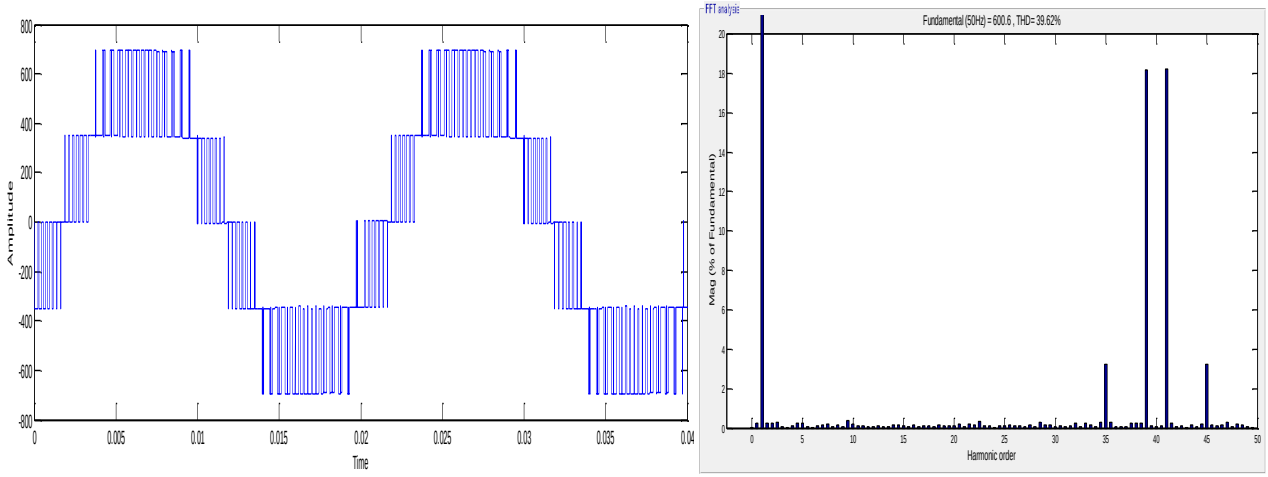

Fig. 4.1 Line Voltage and its Harmonic Spectrum with PD SPWM Technique

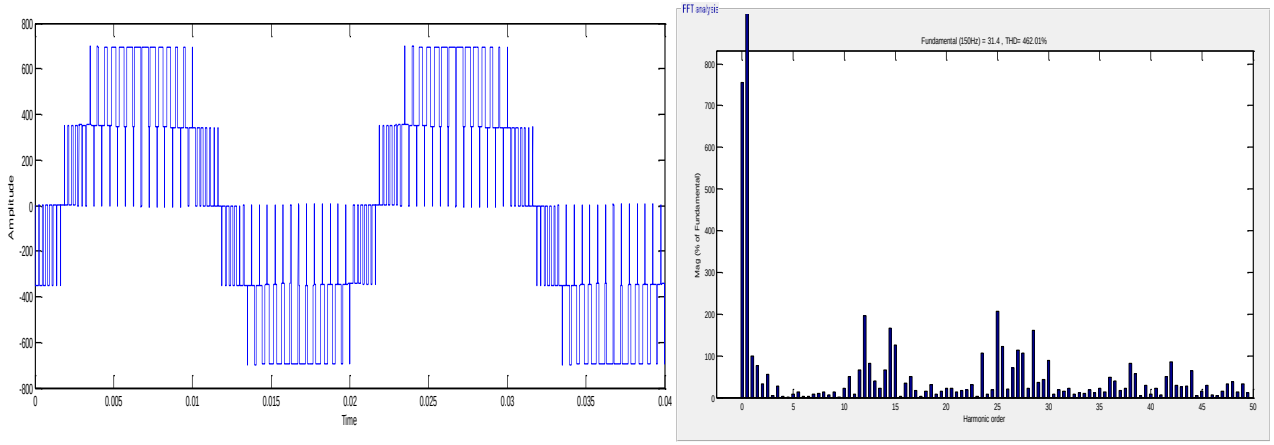

Fig. 4.2 Line Voltage and its Harmonic Spectrum in POD SPWM Technique

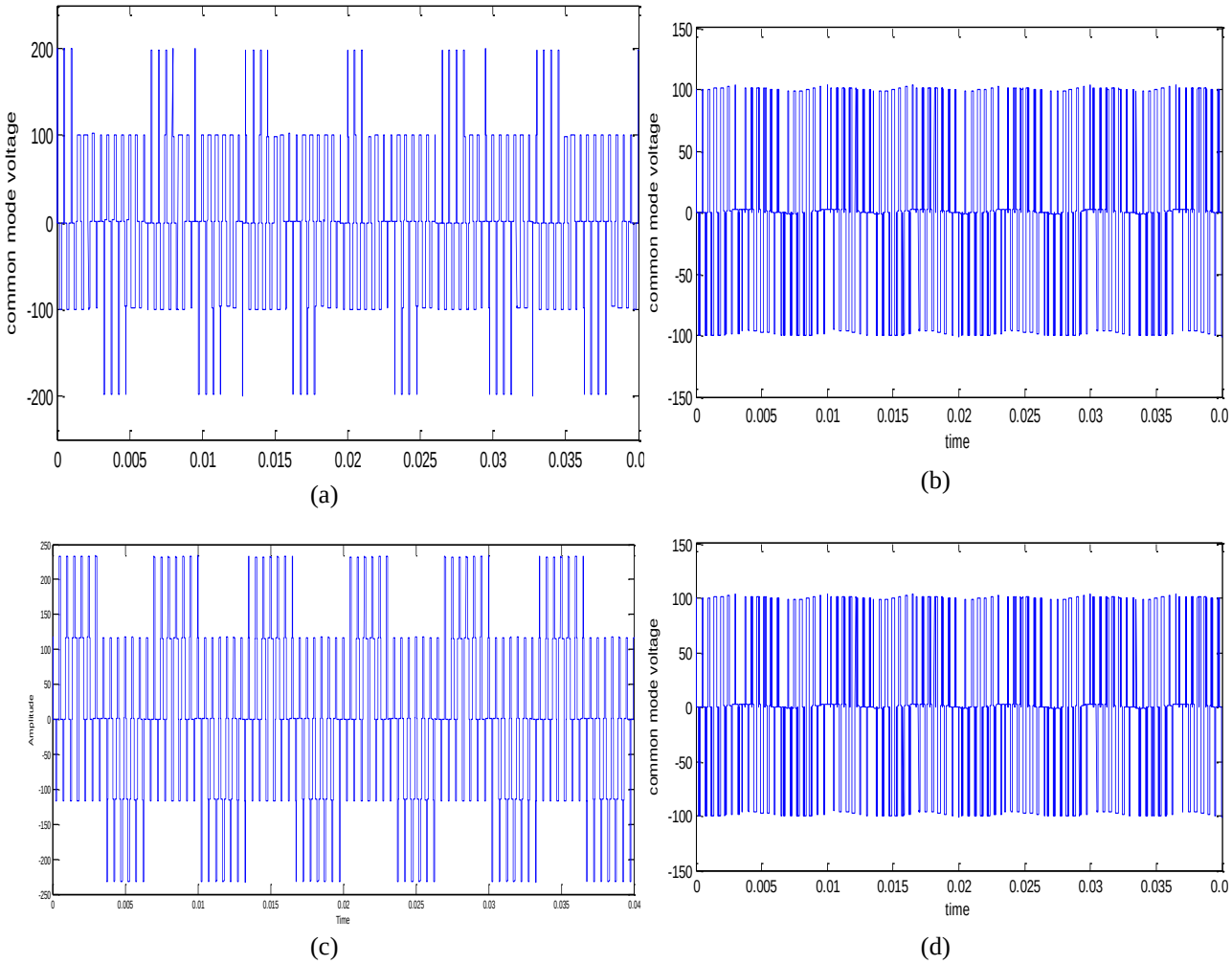

Fig. 4.3 Common Mode Voltages with (a) PD (b) POD (c) Offset Addition of PD technique (d) Offset Addition of POD Technique

CONCLUSIONS

Common mode voltage generated in PWM inverter output may damage the motor windings, shaft, and bearings. Although, some methods have been developed for completely eliminating common mode voltages (with space vector PWM techniques) which is very complex to implement, it may be possible control it via simple SPWM techniques and their modified forms such as addition of common mode voltage offset to the actual reference voltage wave as presented in this paper. Simulation results show that modified SPWM technique not only controls the THD in output voltage of inverter but also reduces the amplitude, switching transients and frequency of common mode voltages. Simple closed loop PI voltage regulator has been proposed to control neutral point potential without sensing dc capacitor voltages.

APPENDIX-I: SIMULATION PARAMETERS

Load: 50 kW, 1 kVAr (inductive), 400 volts, 50 Hz. Source: 3-phase, 10 MVA, 11kV, 50 Hz. Step Down Transformer: 10 MVA, 50 Hz, 11kV/400 Volts. Inverter Output LC Filter: 50 mH, 1 kVar (capacitive). (Open loop), and 2mH, 2kVar (closed loop PI regulator) Voltage Regulator Gains: Kp = 0.1, Ki = 10. Switching Frequency: 2 kHz.

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