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DESIGN OF CHANNEL LENGTH MODULATION FREE MOS TRANSISTOR

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Abstract- Recent days, MOS technology is dominating over BJT technology with its unique advantage of scaling towards lower technologies. This advantage is more suitable to design digital ICs with good accuracy in lower technologies. But, design of analog ICs in lower technologies with good accuracy is limiting due to the poor drain current versus drain-to-source voltage characteristics. These characteristics are deviating much compared with the ideal MOS characteristics due to finite channel length modulation. The prime aim is to minimize or eliminate this channel length modulation by designing suitable circuit techniques including MOS transistor, capacitor, resistor, diode etc. Once we can achieve this ideal characteristics of MOS Transistor, it opens an era to design analog and mixed signal ICs in lower technologies with good accuracy.

Index Terms-Channel length modulation, drain current, MOS transistor, output resistance, scaling

1. INTRODUCTION

One of the short channel effects in MOS transistors is Channel length Modulation[2], which is the major parameter that limits the ideal performance of MOSFET'S[4]. It is due to the difference between drawn length[6] and an effective length. Channel length modulation mainly occurs due to an increase in drain voltage[8], as drain voltage increases the drain depletion width[9] tends to increase as drain and body junction is in reverse bias, which makes the effective channel length decrease when compared to drawn length. As a result the drain current increases which in turn reduces an output resistance.

The output resistance of the MOS transistor can be increased in two ways, one is increasing the substrate doping density[1] which is done at device level during fabrication process and the other is designing a circuit which consists of multiple MOS transistors and linear elements at the circuit level which mimics the exact behaviour of MOS transistor.

As scaling increases towards the lower technology, the channel length modulation parameter increases. This effect typically increases in small nano scale devices[3] with low-doped substrates[5]. This has become a major limitation in a MOSFET era. It can be overcome by proper scaling which can reduce channel length modulation parameter.

2. RELATED WORK

On decreasing the gate length to nano level or even smaller, the gain of the circuits is reduced. We can overcome this by cascoding the transistors resulting in a high gain and good accuracy.

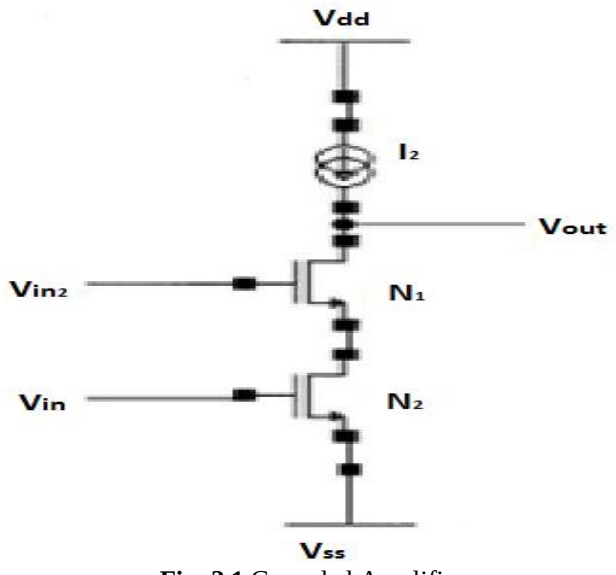

Fig. 2.1 Cascaded Amplifier

$$Av = \frac{v_{out}}{v_{in}} = -g_m R_d \quad 2.1$$

The various ways to increase the gain of the circuit viz.. one among them is to increase the trans conductance (g_m) of the circuit and the other one is to increase the output resistance of the circuit.

Transconductance, $$g_m = \frac{v_{out}}{v_{in}} \quad 2.2$$

Output resistance, $$r_o = \frac{1}{\lambda I_d} \quad 2.3$$

2.1 Super 3T MOS

One of the easiest technique in super MOS transistors is Super 3t MOS[7]. It consists of 3 transistors and an external current source[10]. When super MOS is in saturation region, its characteristics are flat when compared to general NMOS which has bend in it. The improved super 3t MOS differs from super 3t MOS having a current mirror which allows the circuit to self bias as shown in Fig 2.2 and simulation results are shown in Fig 2.3.

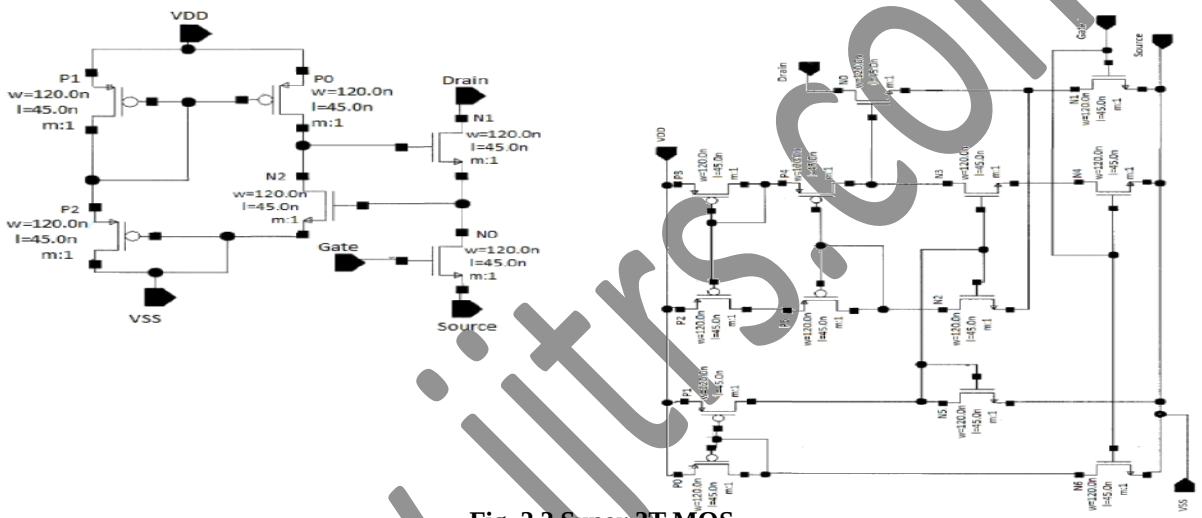

Fig. 2.2 Super 3T MOS

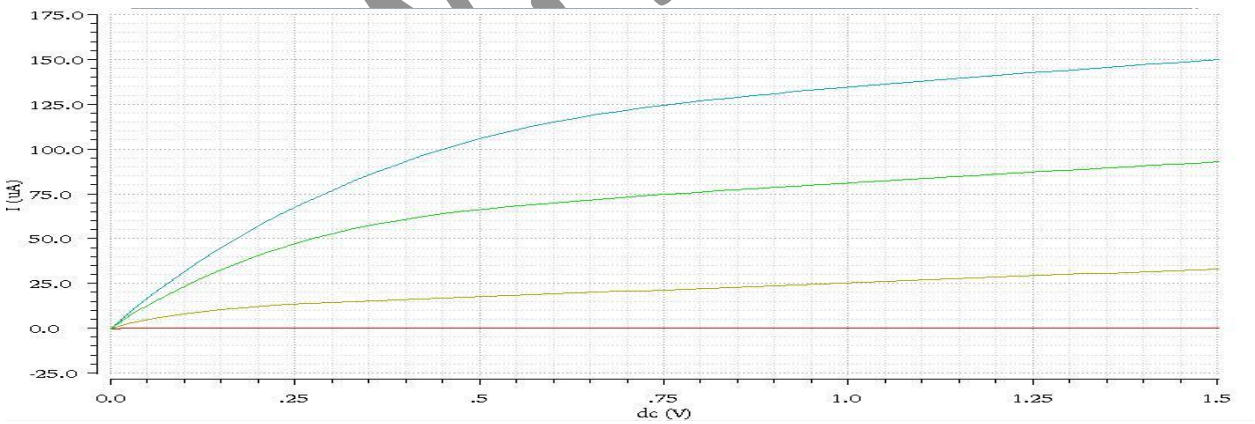

Fig. 2.3 Super 3T MOS Simulation Result

2.2 Super 13T MOS

As the name suggests that there are 13 MOS[8] transistors which are connected in the circuit as shown in Fig 2.4. This circuit mainly comprises of the combination of both PMOS and NMOS current mirrors[9]. The main purpose of keeping this respective current mirrors are in order to acquire the same current with respect to both input as well as output of that particular part of the circuit. There are some limitations of super 13t over super 3t MOS viz.. namely an increase in complexity, an increase in power consumption, and an increase in area. The circuit is shown as in Fig 2.4 consists of namely a biasing stage, a transresistance amplifier and a cascade output [10].

Six transistors are connected to perform the operation of transresistance amplifier namely N_2, N_3, P_2, P_3, P_4, P_5. Transistor N_1 is current limiting factor for the drain current. The biasing of N_1 can be determined by the overdrive voltage of N_0.Fig 2.5. Demonstrates the simulation results of 13t MOS transistor.

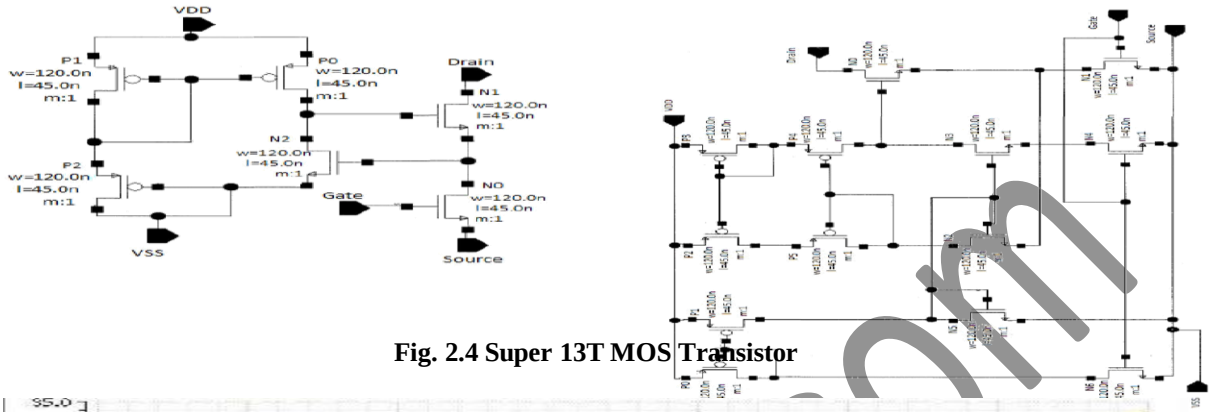

Fig. 2.4 Super 13T MOS Transistor

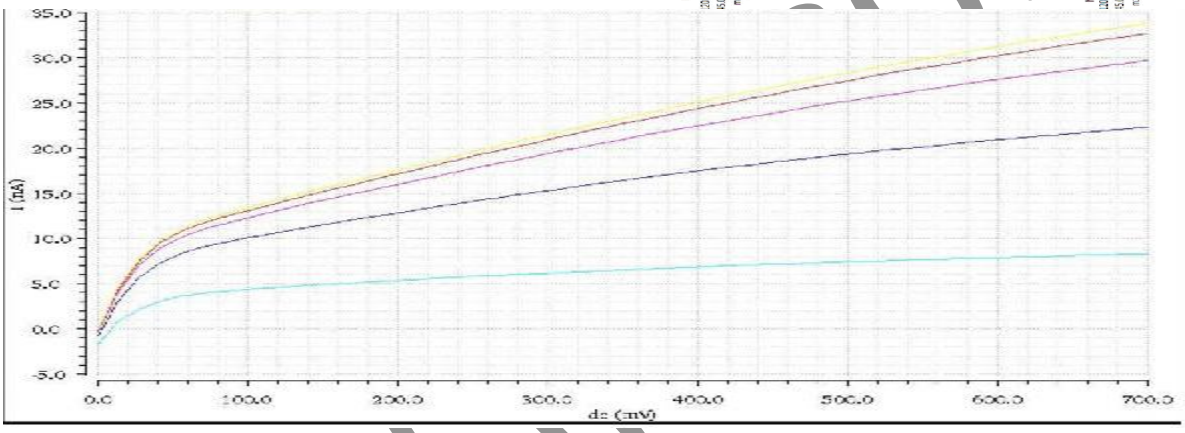

Fig. 2.5 .Super 13T MOS Simulation Result

3. PROPOSED TECHNIQUE

The basic idea behind the proposed technique is to cancel the positive slope of drain current characteristic curve in saturation region by employing the circuit which induces negative slope. If we glance the MOS Characteristics curve, we are obtaining a positive slope which was supposed to remain constant in order to minimize the parameter. So, by inducing negative slope curve in saturation region of MOS drain characteristics will result in adding up of positive and negative slope of both curves resulting a constant straight line.The Fig 3.1 gives a view of our proposed technique and Fig. 3.2 gives an idea about the characteristics obtained after considering circuit shown in Fig 3.1.

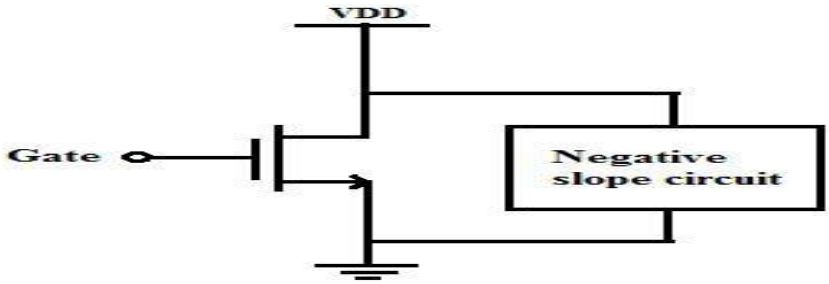

Fig 3.1 A Basic Approach for Proposed Technique

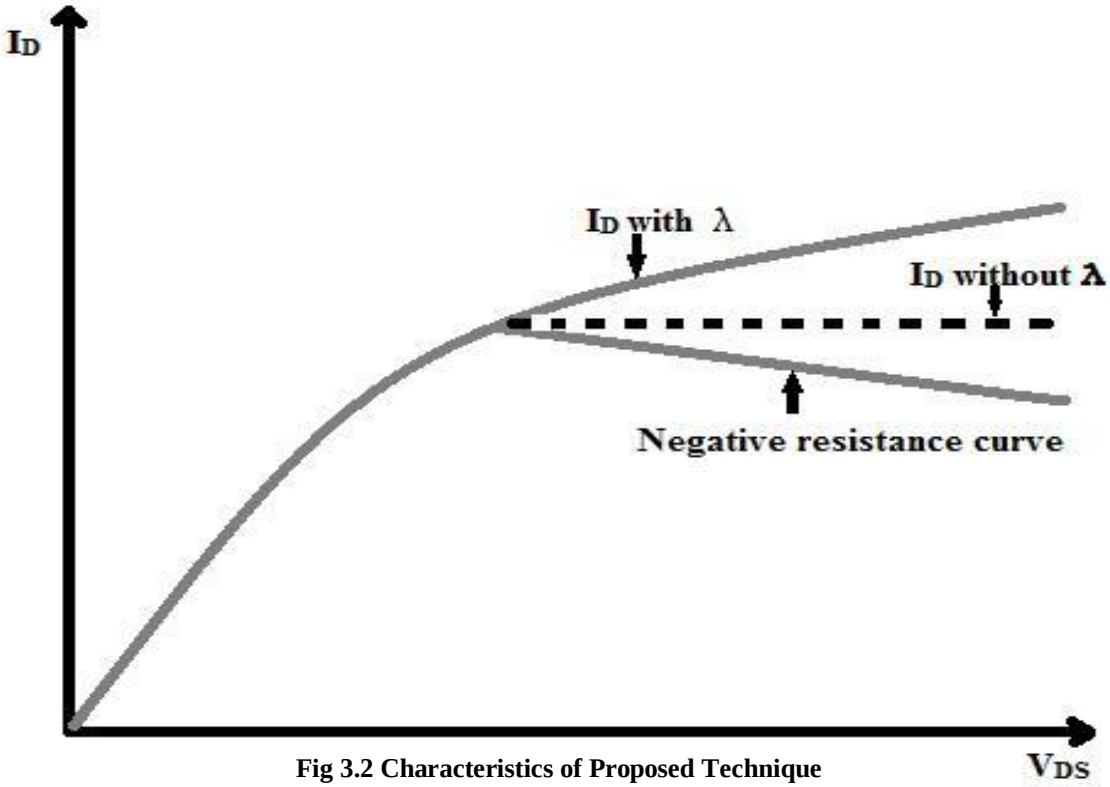

Fig 3.2 Characteristics of Proposed Technique

3.1 Negative Resistance MOS Circuits

A combination of MOS transistors and linear resistors can exhibit negative resistance. There are many circuits using MOS that can exhibit negative resistance. One such combination is NMOS cross coupled circuit which exhibit negative resistance of $-1/g_m$ which was shown in Fig 3.3

$$R_{out} = \frac{r_{out}}{1-g_m r_{out}} R \qquad 3.1$$

$_{OUT}$: Output impedance of MOS transistor by proposed technique.

r_{out} : Output impedance of normal MOS transistor.

g_m : Trans-conductance.

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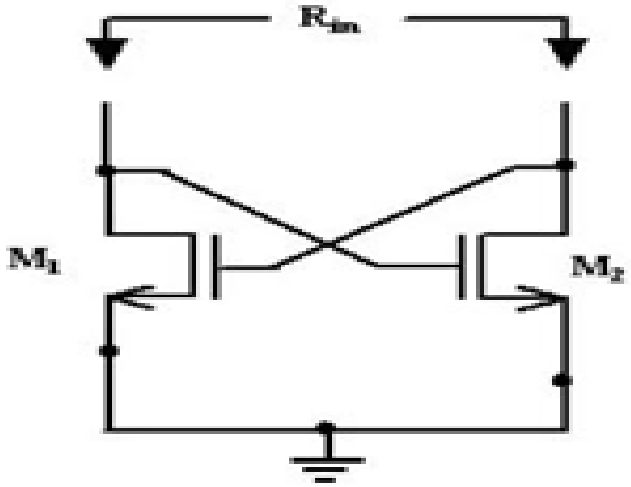

Fig 3.3 NMOS Cross Coupled Circuit

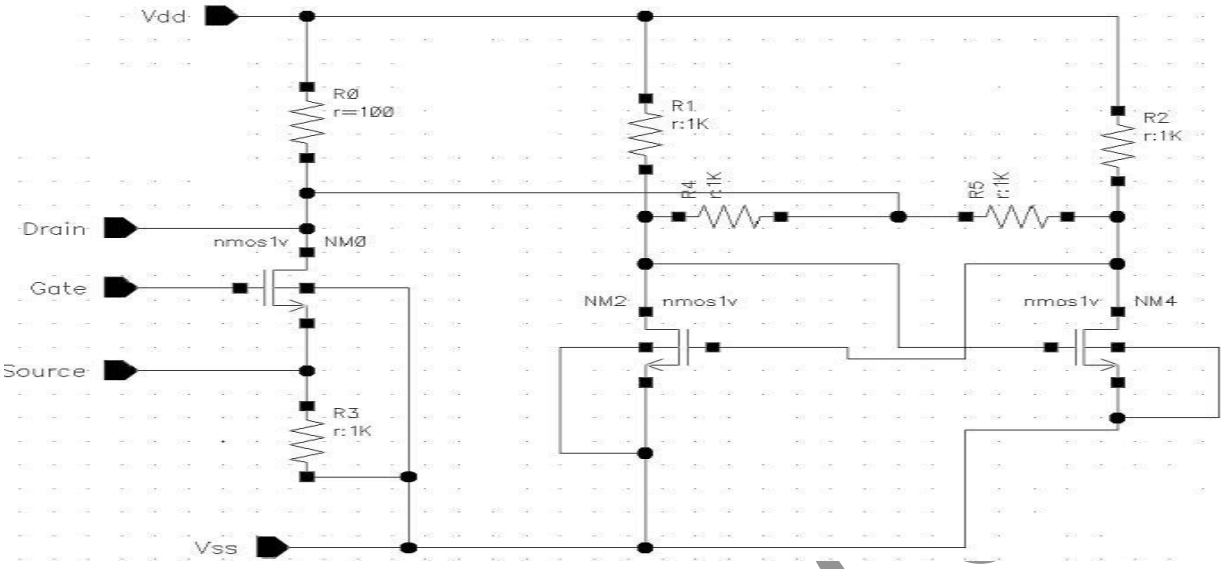

Fig 3.4. Schematic Circuit of Proposed Technique Utilizing Slope Cancellation Technique.

In the Proposed technique, MOS negative resistance circuit is connected across the drain terminal of normal MOS transistor (NM0) .The drain current of NM0 MOS transistor is drawn by the negative resistance circuit. The resistance R_0 and R_3 are used for biasing the NM0 MOS transistor. All the MOS transistors in the negative resistance circuit are to be operated in saturation region. Three terminals are drawn out of the entire circuit which acts as drain, source and gate of the new implemented MOS transistor as shown in Fig 3.4.This entire circuit will behave as a MOS transistor with reduced λ and increased output impedance.

4. SIMULATION RESULTS

The Simulation results for our proposed technique are demonstrated in Fig. 4.1 using the cadence virtuoso tool .It can be easily seen the effectiveness of our method in reducing the channel length modulation.The results shown in Table 4.1 gives clearly the improvement of our design over super 3t MOS circuits and Super 13t MOS circuits.

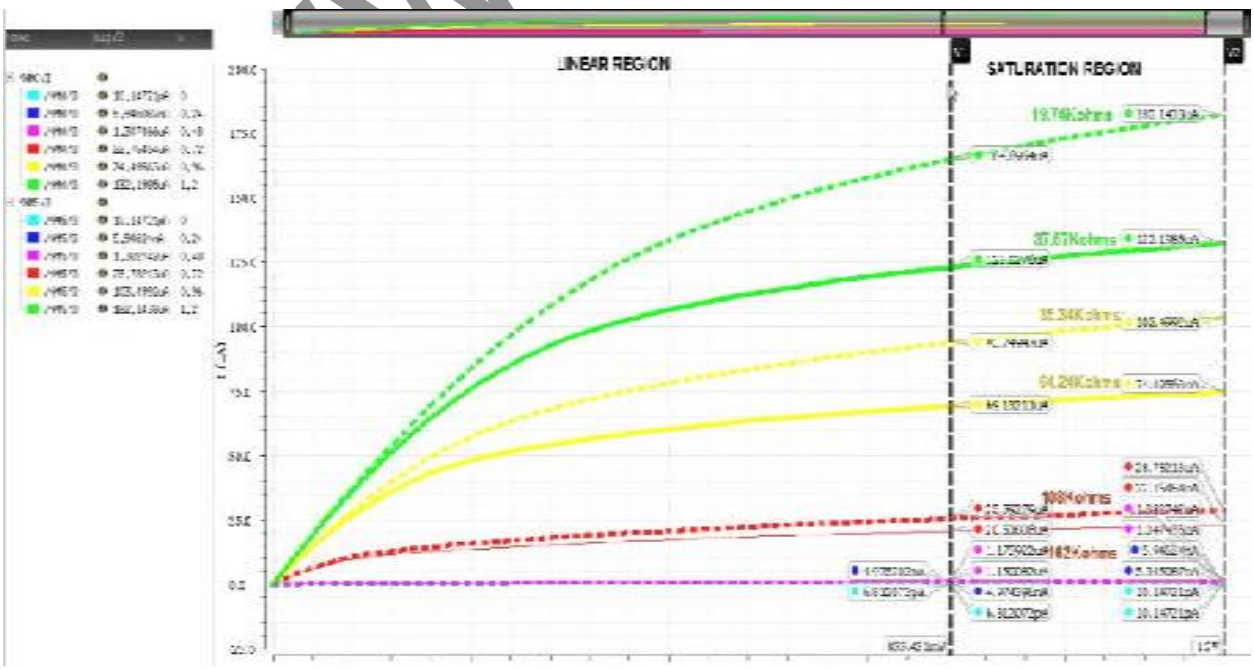

Fig 4.1. Simulation Results

These values are tabulated at Vgs=0.96v.

Table -4.1 Comparison of Techniques

Parameter	Super 3t	Super 13t	Negative resistance circuit
λ in saturation	0.26 V^{-1}	0.12V^{-1}	0.03 V^{-1}
r_0 in saturation	25.44kΩ	38.12kΩ	64.24kΩ

5. CONCLUSION

MOSFET is an incredible device which has opened a gateway to a new leading era and has wide number of applications when compared to BJT. One of the parameters affecting the ideal behaviour of the MOSFET is channel length modulation parameter. Minimizing this parameter can make MOSFET to perform at its best performance. In this paper we have compared the characteristics of both super 3t and super 13t in terms of their output resistance and respective parameters as it is tabulated, which is not at all approximate to achieve the best characteristics of the MOSFET. Hence, through this paper we have introduced a new technique called the slope cancellation technique which may minimize the effect of channel length modulation parameter. If this approach has to be utilized in future, then it might be a great boon for circuit designers. The greatest advantage of using this method is to maximize the output resistance and to minimize the channel length modulation parameter and ultimately achieved our target while designing a channel length modulation free MOS transistor.

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