ISSN No.: 2454- 2024 (online)

International Journal of Technical Research & Science

EFFICIENT DESIGN OF LOW POWER MULTIPLIER USING MHNG REVERSIBLE LOGIC GATE

Ankush[1], Sonam[2]
E-mail Id: amongia9@gmail.com[1], sonam.mongia8@gmail.com[2]
[1]M.Tech, Department of ECE, Punjabi University, Patiala, Punjab (India)
[2]M.C.A Department of Computers, Kurukshetra University, Kurukshetra, Haryana (India)

Abstract- Low power VLSI circuit design is one of the most important issues in present day technology. One of the ways of reducing power is to use the reversible technology. Reversible logic has received great importance in the recent years because of its feature of reduction in power dissipation. It finds applications in low power digital designs, quantum computing, nanotechnology, DNA computing etc. Large number of researches are currently ongoing on sequential and combinational circuits using reversible logic. Multiplier is one of the most important circuits used in combinational logic. In this article, we have proposed an efficient design of 8-bit Multiplier using MHNG and Peres reversible logic gates. In order to show the efficiency, lower bounds of the proposed designs are shown in terms of power consumption and quantum cost needed.

Index Terms- Reversible Logic Gates, Reversible Multiplier Circuit, Quantum Computing, Power Consumption.

1. INTRODUCTION

The logical classic gates such as AND, XOR, NOT, and OR cannot predict the existent inputs by assuming the outputs, so they will lose a lot of information. Loss of information increases heat and finally leads to wasting energy. If we can produce the outputs from the inputs and obtain the inputs from their correspondent outputs, no energy will be lost and this property can be seen in reversible logic.

The electronic industry faced a greater challenge to decrease the energy dissipation of circuits along with the wide advancements in the era of integrated circuits. The above fact is the main reason for designing reversible logic gates for reducing the power dissipation which in recent years has gained greater momentum.

According to the principle of Landauer (1961), the conventional combinational logic circuits dissipate energy due to the information loss in the process. The energy dissipation of KTln2 joules occurs for each bit of information where K is the Boltzmann's constant of 1.38×10-23 J/K and T is the absolute temperature at which the computations are performed. This dissipation has got greater impact on the life and speed of CMOS devices. Many researchers demonstrated that the energy dissipation can be kept under control by the introduction of reversible logic gates.

A reversible logic gate is a k-input and k-output device (denoted k*k) where inputs must be equal to its outputs. Reversible gate can generate unique output pattern for each input vector and vice versa i.e., there is correlation between each of its input and output assignment. Since the usage of fan outs are disallowed in the reversible logic circuits, additional logic gates can be introduced in order to achieve the required result.

2. BASIC RULES AND PROPERTIES IN REVERSIBLE LOGIC

In designing reversible circuits, the following important rules and properties are observed:

2.1 Lack of Fanout

In designing reversible circuits, an extension of a given line is not allowed. In addition, any loop should not be present in reversible circuits [4].

2.2 The Least Number Of Reversible Gates

The whole number of reversible gates used in a circuit is called the number of reversible gates; the least number of these gates results in optimal reversible circuits [5].

2.3 The Least Number of Garbage Outputs

Outputs that are not used in reversible circuit computations but are used in the circuit for the purpose of equality of input numbers with those of outputs are called garbage outputs the least number of garbage outputs results in optimal reversible circuit

2.4 The Least Number of Constant Inputs

Inputs that are added to an n * m function in order to change this function into a reversible one are called constant inputs [7]. The least number of constant inputs results in optimal reversible circuits.

2.5 Minimizing the Quantum Cost

Quantum cost of reversible circuits is defined by the number of 1 * 1 or 2 * 2 gates used in the circuit, and all of the 1 * 1 and 2 * 2 reversible gates have quantum costs equal to one. Quantum cost of a gate is obtained by counting the number of 1 * 1 and 2 * 2 reversible gates; therefore, the least number of these gates would have the least cost and, consequently, we will have better reversible circuits.

3. LITERATURE SURVEY

Thapliyal and Rang Nathan [5] proposed the design of Reversible Binary Sub tractor using TR Gate. The particular function like Binary Subtraction is implemented using TR gate effectively by reducing number of Reversible gates, Garbage outputs and Quantum Cost. Thapliyal and Ranganathan [6] presented a design of Reversible latches viz., D Latch, JK latch, T latch and SR latch that are optimized in terms of quantum cost, delay and garbage outputs. Lihui Ni et al., [7] described general approach to construct the Reversible full adder and can be extended to a variety of Reversible full-adders with only two Reversible gates. Irina Hashmi and Hafiz Hasan Babu [8] designed an efficient reversible barrel shifter which is capable of left shift/rotate used for high speed ALU applications.

Robert Wille et al., [9] explored two techniques from irreversible equivalence checking applied in the reversible circuit domain. (i) Decision diagram Technique equivalence checking for quantum circuits and (ii) Boolean satifiability checking for garbage input/outputs. Noor Muhammed Nayeem et al., [10] presented designs of Reversible shift registers such as serial-in serial-out, serial-in parallel-out, parallel-in serialout, parallel-in parallel-out and universal shift registers. Majid Mohammadi, Mohammad Eshghi et al., [11] proposed a synthesis method to realize a Reversible Binary Coded Decimal adder/subtractor circuit. Genetic algorithms and don't care concepts used to design and optimize all parts of a Binary Coded Decimal adder circuit in terms of number of garbage inputs/outputs and quantum cost.

Majid Mohammadi and Mohammad Eshghi [12] explained about the behavioral description and synthesis of quantum gates. To synthesize reversible logic circuits, V and V+ gates are shown in the truth table form and shown that bigger circuits with more number of gates can be synthesized. Rekha James et al. [13] proposed an implementation of Binary Coded Decimal adder in Reversible logic, which is basis of ALU for reversible CPU.

VLSI implementations using one type of building block can decrease system design and manufacturing cost. Himanshu Thapliyal and Vinod [14] presented the Transistor realization of a new 4*4 Reversible TSG gate. The gate alone operates as a Reversible full adder. The Transistor realizations of 1-bit Reversible full adder, ripple carry adder and carry skip adder are also discussed. Himanshu Thapliyal and Srinivas [15] proposed a 3x3 Reversible TKS gate with two of its outputs working as 2:1 multiplexer. The gate used to design a Reversible half adder and further used to design multiplexer based Reversible full adder. The multiplexer based full adder is further used to design Reversible 4x4 Array and modified Baugh Woolley multipliers

In 2016, Ankush et al. described that the reversible modified Fredkin gates and modified HNG gates can be used to design the Carry Skip adder with low quantum cost. The quantum cost and the power dissipation of proposed carry skip adder design using modified Fredkin gates was reduced as compared to existing carry skip adder using Fredkin gate [16].

In 2016, Ankush et al. proposed different types of reversible residue adders using modified Fredkin gates and modified TSG gates. Various parameters of reversible circuits such as, quantum cost and power dissipation of proposed reversible residue adders were reduced as compared to previous designs. The reversible logic circuits can also be designed with less area and delay [17].

In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss lover the last decades. The power dissipation in a circuit can be reduced by the use of reversible logic.

4. REVERSIBLE LOGIC GATES

The following classification gives the reversible logic gates used in our proposed circuit -

4.1 Peres Gate (PG)

The 3×3 Peres gate is designated as follows: Input vector Iv = (A, B, C) and output vector Ov= (P=A, Q=A⊕B, R=AB⊕C). Block diagram of Peres is showed in Fig. 4.1 Peres gate is the combination of Feynman gate and Toffoli gate and this can contrivance operations like AND EX-OR. The quantum cost of PG gate is 4 [15].

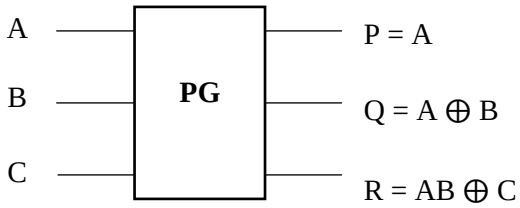

Fig. 4.1 Peres Gate

4.2 MHNG Gate

MHNG gate is a 4x4 reversible gate with following input and output vectors, Iv = (A, B, C, D) and Ov = (P = A, Q = D, R = A⊕B⊕C, S = (A⊕B).C⊕AB⊕D. One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit. The quantum cost of MHNG gate is 5.

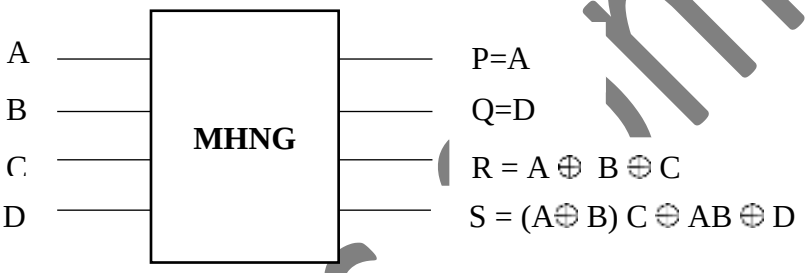

Fig. 4.2 MHNG Gate

5. PROPOSED WORK

Multipliers play a key role in the high performance digital systems. Multipliers are key components of many high performance systems such as FIR filters, Microprocessors, Digital Signal Processors, ALU etc. A system's performance is generally determined by the performance of the multiplier as the multiplier is generally the slowest element in the system and generally consumes more area and power and long latency. Therefore, low-power multiplier design has been an important part in low-power VLSI system design.

MHNG gates and PGs are used in the design of the 8-bit reversible multiplier [11]. It is having two phases to perform multiplication. In the first phase, the partial products are generated in parallel using PG as shown in fig. 5.1. Here X and Y are inputs, the output contains both partial products and garbage's. In the second phase, the addition of partial products is performed using reversible half-adder and full-adder gates constructed using the PG and HNG gate as shown in figure 4. The multiplier produces the product P (P0 to P7) for the inputs x and y.

The basic cell for such a multiplier is a full adder (FA) accepting three bits. We use MHNG gates as reversible full adder which is depicted in Figure 4. The proposed reversible multiplier circuit uses eight reversible MHNG full adders. In addition, it needs four reversible half adders. It is possible to use MHNG gate as half adder, but we use Peres gate as reversible half adder because it has less hardware complexity and quantum cost compared to the MHNG gate.

			x	x_3	x_2	x_1	x_0
				y_3	y_2	yx_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig. 5.1Partial Product Generation of x & y Inputs

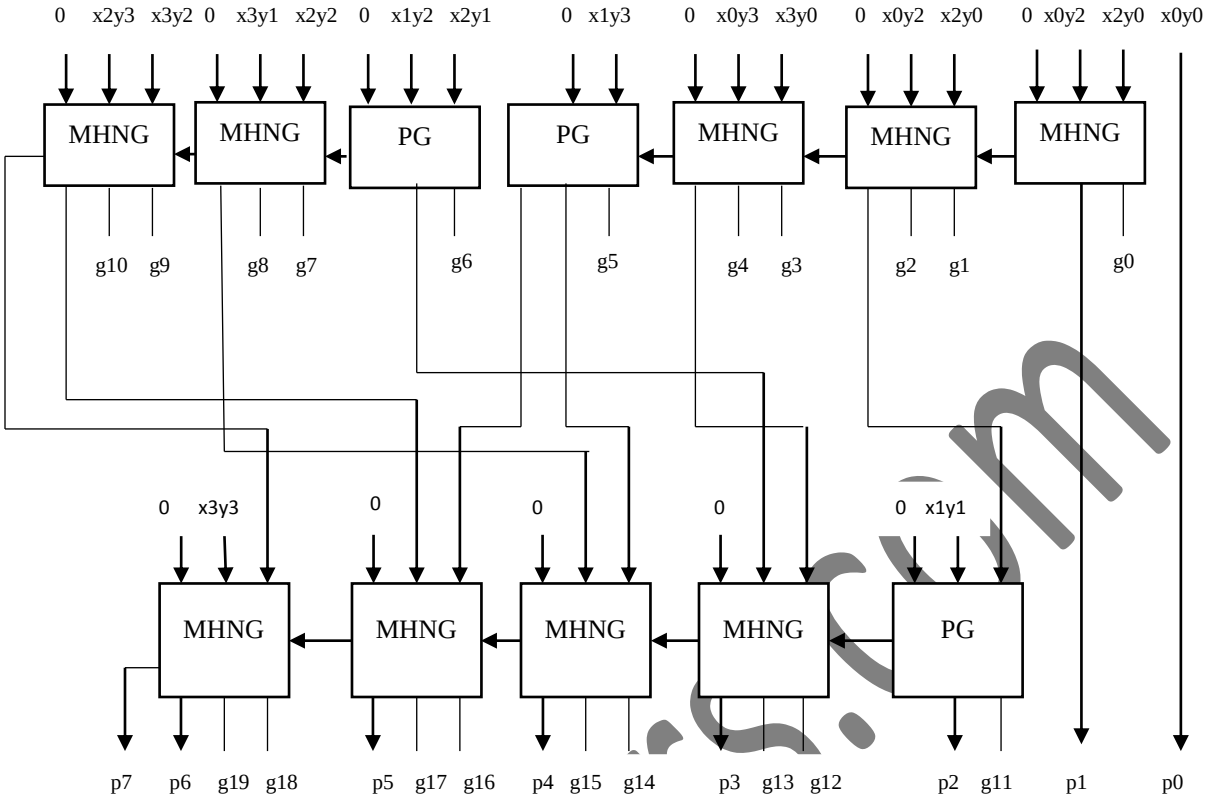

Fig. 5.2 Proposed 8-bit Design of Reversible Multiplier Circuit

The fig. 5.2 shows the proposed design of 8-bit multiplier circuit using MHNG and Peres reversible logic gates. It uses 3 peres gates and 9 MHNG gates. The circuit produces 19 garbage outputs and having 12 constant inputs which are marked as 0. The quantum cost of MHNG gate is 5 whereas the quantum cost of HNG gate is 6. Thus the proposed circuit reduces quantum cost of the circuit.

TOTAL QC = 3 QC (PG) + 9 QC (MHNG)

= 12 + 45

= 57

6. IMPLEMENTATION & RESULTS

Table-6.1 Comparison of Proposed Work with Existing Work

Multiplier Circuit	Quantum Cost	Power Consumption (W)
Proposed Design	57	3.962 W
Existing Design [18]	66	5.360 W

7. SIMULATION METHODOLOGY

The fig. 7.1 shows the RTL schematic of top module for reversible 8-bit multiplier circuit using PG & MHNG reversible logic gates. It contains inputs x and y as input vectors and Cin is the input carry. The Cout & P are the outputs, P which contains 8 bits (P0- P7).

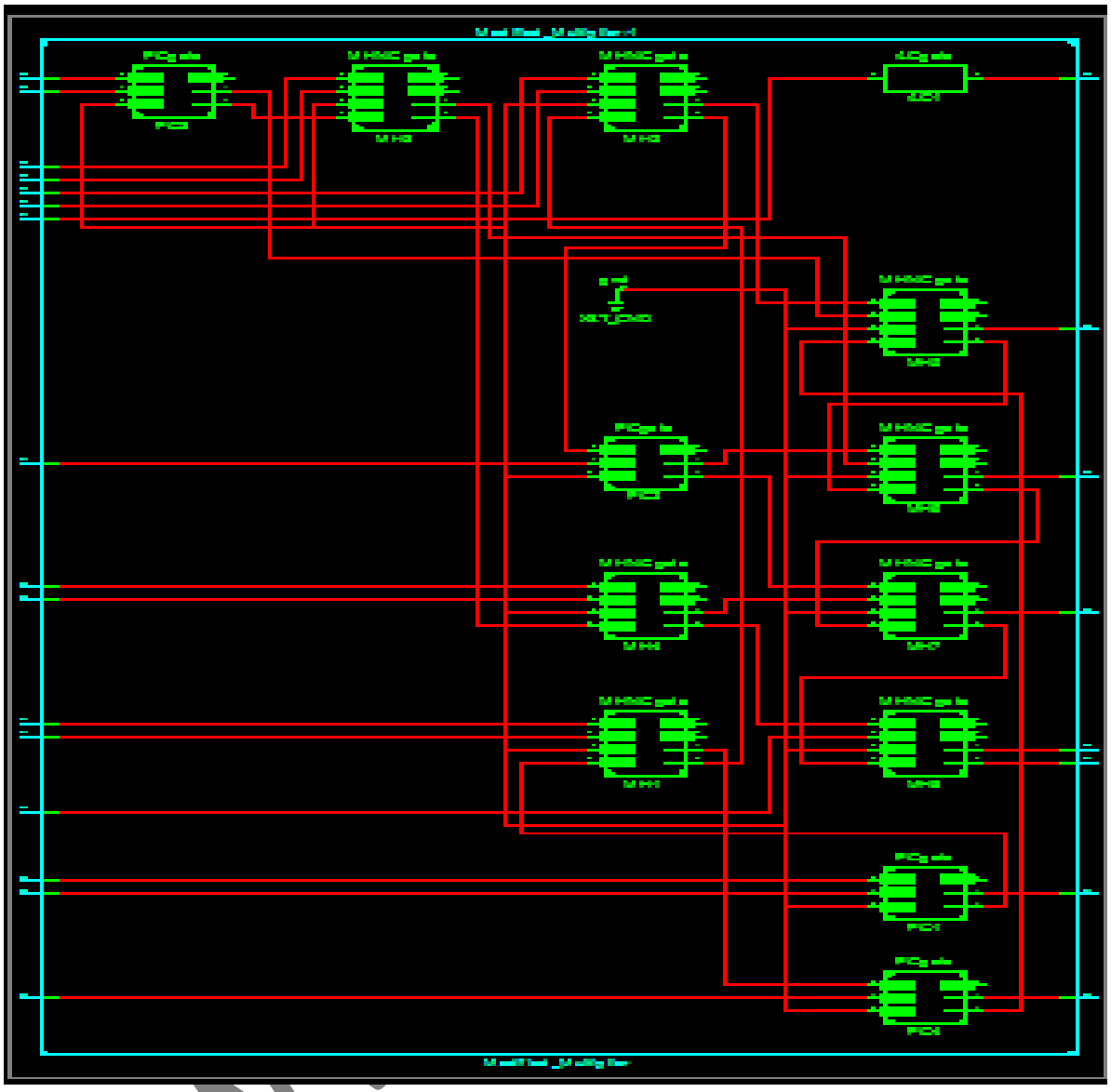

Fig. 7.1 RTL View of Proposed 8-bit Design of Reversible Multiplier Circuit

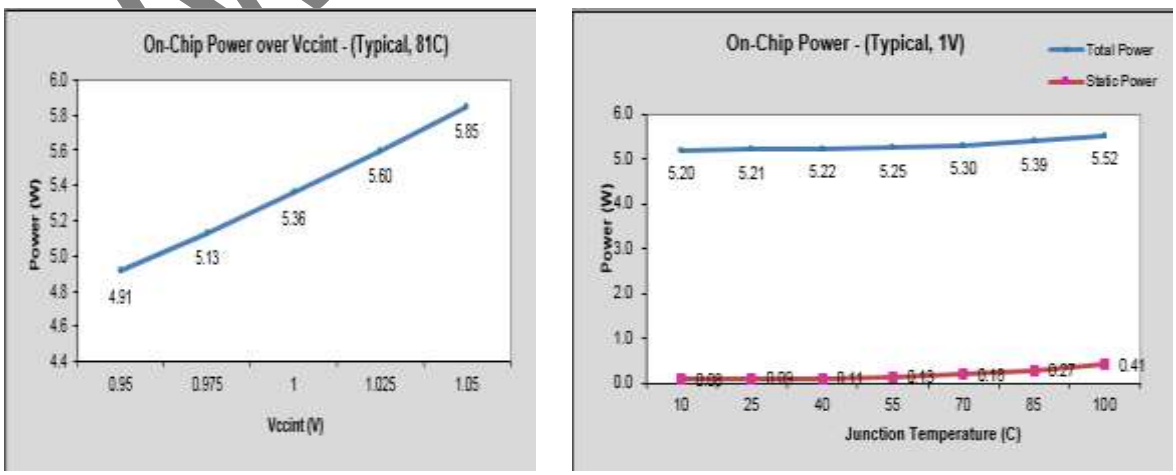

Fig. 7.2 Power Consumption Graph of Existing 8-bit Reversible Multiplier Circuit [18]

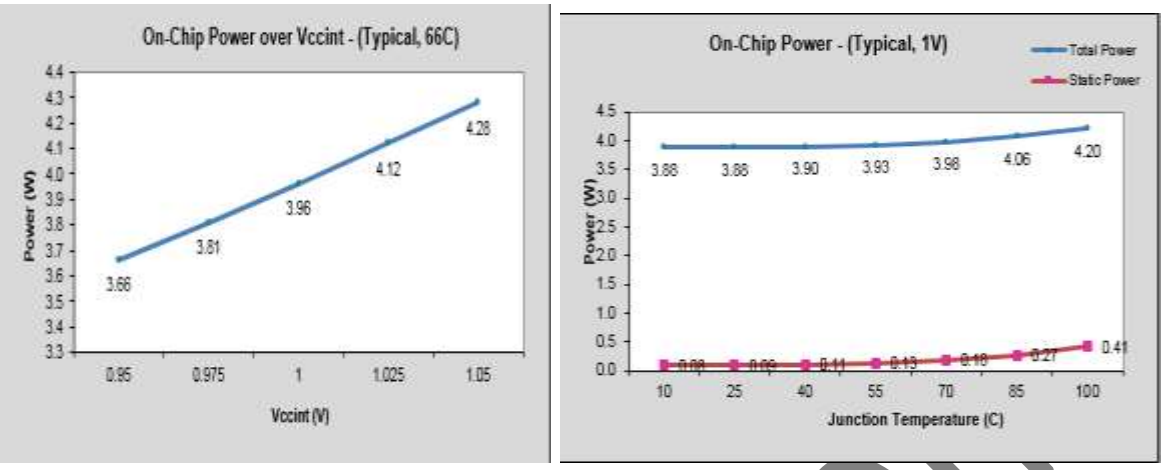

Fig. 7.3 Power Consumption Graph of Proposed 8-bit Reversible Multiplier Circuit

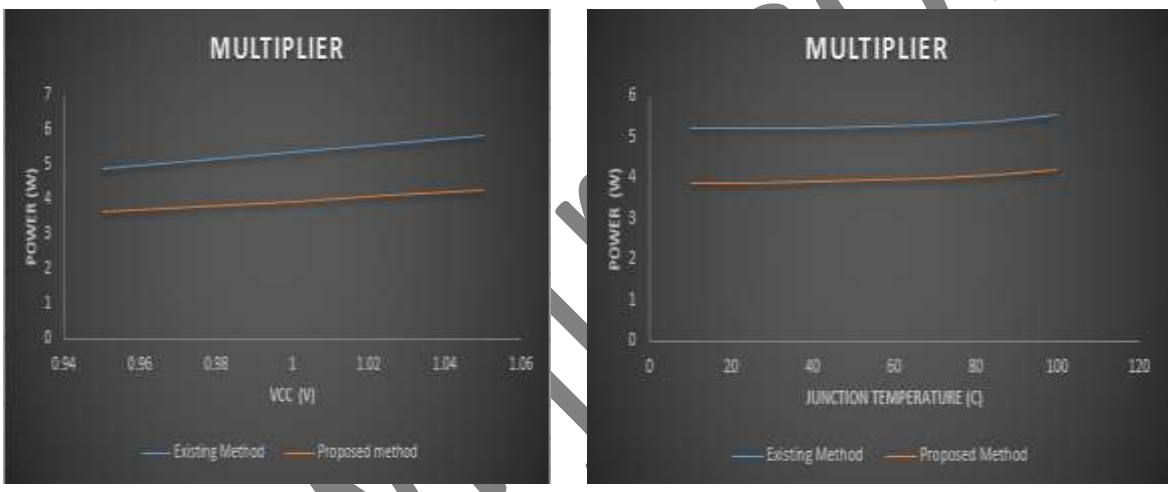

Fig. 7.4 Comparative Results of Power Consumption Graph for Proposed & Existing 8-bit Reversible Multiplier Circuit [18]

In the fig. 7.8 the graph between the Vcc and Output Power shows that the proposed design consumes 3.96 watt of power while the existing design consumes 5.36 watt of power. Similarly the graph between the Junction Temperature and Output Power shows that the proposed design consumes 3.96 watt of power while the existing design consumes 5.36 watt of power.

8. CONCLUSION & FUTURE WORK

Reversible computing has its great significance in diminishing the complexity of the digital circuits. In this paper, reversible logic synthesis were carried out for 8 bit reversible multiplier circuit. Table 1 demonstrates that the proposed 8 bit reversible multiplier circuit is better than the existing designs in terms of power consumption and quantum cost. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology and can be further design for 16 bit, 32 bit and 64 bit.

REFRENCES

[1] Landauer.R “Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2] Bennett C H “Logical Reversibility of Computation”, IBM J.Research and Development, pp. 525-532, November 1973.

[3] Majid Mohammadi, Mohammad Eshghi, Abbas Bahrololoom,"" Behavioral Model of V and V+ Gates to Implement the reversible Circuits Using Quantum Gates"", IEEE, 2008.

[4] D. Michael Miller and Zahra Sasanian, "" Lowering the Quantum Gate Cost of Reversible Circuits"", IEEE, 2010.
[5] H Thapliyal and N Ranganathan, (2009) "Design of Efficient Reversible Binary Sub tractors Based on a New Reversible Gate", IEEE Proceedings of the Computer Society Annual Symposium on VLSI, pp. 229-234.
[6] H Thapliyal and N Ranganathan, (2010) "Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs", Proceedings of Twenty Third International Conference on VLSI Design, pp. 235-240.
[7] Lihui Ni, Zhijin Guan, and Wenying Zhu, (2010) "A General Method of Constructing the Reversible Full Adder", Third International Symposium on Intelligent Information Technology and Security Informatics, pp. 109-113.
[8] Irina Hashmi and Hafiz Md. Hasan Babu, (2010) "An Efficient Design of a Reversible Barrel Shifter", Twenty Third International Conference on VLSI Design, pp. 93-98.
[9] Robert Wille, Daniel Grobe, D Michael Miller, and Rolf Drechsler, (2009) "Equivalence Checking of Reversible Circuits", Thirty Ninth International Symposium on Multiple-Valued Logic, pp. 324-330.
[10] Noor Muhammed Nayeem, Md. Adnan Hossain, Lafifa Jamal, and Hafiz Md. Hasan Babu, (2009) "Efficient Design of Shift Registers using Reversible Logic", International Conference on Signal Processing Systems, pp. 474-478.
[11] Majid Mohammadi, Mohammad Eshghi, Majid Haghparast and Abbas Bahrololoom, (2008) "Design and Optimization of Reversible BCD Adder/Sub tractor Circuit for Quantum and Nanotechnology Based Systems", World Applied Sciences Journal, vol. 4, no. 6, pp. 787-792.
[12] Majid Mohammadi and Mohammad Eshghi, (2008) "Behavioral description of V and V+ gates to Design Quantum Logic Circuits", Fifth International Multi- Conference on Systems, Signals and Devices, pp. 1-6.
[13] Rekha K James, Shahana T K, K Poulose Jacob, and Sreela Sasi, (2007) "A New Look at Reversible Logic Implementation of Decimal Adder", the International Symposium on System-On-Chip.
[14] Himanshu Thapliyal and A P Vinod, (2006) "Transistor Realization of Reversible TSG Gate and Reversible Adder Architectures", Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, pp. 418- 421.
[15] Himanshu Thapliyal and M B Srinivas, (2006) "Novel Design and Reversible Logic Synthesis of Multiplexer Based Full Adder and Multipliers", Forty Eight Midwest Symposium on Circuits and Systems, vol. 2, pp. 1593 – 1596.
[16] Ankush, Amandeep Singh Bhandari, "Design & Performance Analysis of Low Power Reversible Carry Skip Adder", IOSR Journal of VLSI and Signal Processing, vol. 6, Issue 4, Ver. II,(2016),pp.33-39
[17] Ankush, Amandeep Singh Bhandari, "Design & Performance Analysis of Low Power Reversible Residue Adder", International Journal of Hybrid Information Technology, vol. 9,Issue 9,(2016),pp.93-102.
[18] Kamaraj Arunachalam, Marichamy Perumalsamy, C. Kalyana Sundaram and J. Senthil Kumar, "Design and Implementation of a Reversible Logic based 8-Bit Arithmetic and Logic Unit". International Journal of Computers and Applications, Vol. 36, No. 2, July 2014
[19] Ankush, Amandeep Singh Bhandari, "Review Paper on Reversible Logic Gate", International Journal for Research in Electronics & Communication Engineering, vol. 1, Issue 7, (2016).
[20] Ankush, Sonam, "An Improved Design of Low Power BCD Adder using Reversible Computing", International Journal of Advance Science & Technology, vol. 104, pp.33-42, (2017).